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UNITED MICROELECTRONICS CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

MICRON TECHNOLOGY, INC.,

Plaintiff,

v.

UNITED MICROELECTRONICS CORPORATION, FUJIAN JINHUA INTEGRATED CIRCUIT CO., LTD., and DOES 1-10,

Defendants.

Case No. 3:17-CV-06932-MMC

DECLARATION OF JOHN BERG IN SUPPORT OF UNITED MICROELECTRONICS CORPORATION'S MOTION TO DISMISS MICRON TECHNOLOGY, INC.'S FIRST AMENDED COMPLAINT FOR LACK OF PERSONAL JURISDICTION

Judge:	Hon. Maxine M. Chesney
Courtroom:	7 – 19th Floor
Hearing date:	
Hearing time:	
FAC Filed:	February 8, 2019

<u>REDACTED</u> VERSION

I, John Berg, declare as follows:

I. BACKGROUND AND QUALIFICATIONS

1. I have been retained by Dan Johnson Law Group LLP, counsel for Defendant United Microelectronics Corporation ("UMC" or "Defendant"), as an expert on dynamic random-access memory ("DRAM") design and semiconductor processing. I have been asked to provide expert opinion testimony to the Court regarding the contention of Micron Technology, Inc. ("Micron") and its expert, David Liu, Ph.D., that the following patents and published patent applications, which are assigned to United Microelectronics Corporation ("UMC") and/or Fujian Jinhua Integrated Circuit Co., Ltd. ("Jinhua"), were "based on" or "derived from" Micron trade secrets:

- U.S. Patent No. 9,679,901 ("'901 Patent") (attached to the Declaration of Douglas L. Clark in Support of Micron's Supplemental Opposition to UMC's Motion to Dismiss ("Clark Decl.") as Exhibit 33);
- U.S. Patent No. 9,773,790 ("'790 Patent") (attached to the Clark Decl. as Exhibit 35);
- U.S. Patent No. 9,859,283 ("'283 Patent") (attached to the Clark Decl. as Exhibit 38);
- U.S. Patent No.` 9,929,162 ("'162 Patent") (attached to the Clark Decl. as Exhibit 36);
- U.S. Patent No. 9,960,167 ("'167 Patent") (attached to the Declaration of Robert G. Litts in Support of Defendant United Microelectronics Corporation's Reply to Plaintiff Micron Technology, Inc.'s Opposition to Motion to Dismiss ("Litts Decl.") as Exhibit 1);
- U.S. Patent No. 10,062,700 ("'700 Patent") (attached to the Declaration of Marcus Quintanilla in Support of Micron's Opposition to Jinhua's Motion to Dismiss ("Quintanilla Decl.") as Exhibit 11);
- U.S. Patent App. Publication No. 2018/0076205 ("'205 Publication") (attached to the Quintanilla Decl. as Exhibit 15);

- U.S. Patent App. Publication No. 2018/0108563 ("'563 Publication") (attached to the Clark Decl. as Exhibit 34);
- U.S. Patent App. Publication No. 2018/0190538 ("'538 Publication") (attached to the Quintanilla Decl. as Exhibit 12);
- U.S. Patent App. Publication No. 2018/0190657 ("'657 Publication") (attached to the Quintanilla Decl. as Exhibit 14); and
- U.S. Patent App. Publication No. 2018/0197863 ("'863 Publication") (attached to the Quintanilla Decl. as Exhibit 13).

I will herein refer to these patents collectively as the "UMC/Jinhua Patents." I base the opinions contained in this declaration on my education and professional experience in the semiconductor industry, and on my study of the following documents and information: the UMC/Jinhua Patents; other issued patents and published patent applications relating to DRAM design and semiconductor processing technology; reverse-engineering reports prepared by non-party companies such as Chipworks Inc. ("Chipworks") and TechInsights Inc. ("TechInsights"); materials relating to DRAM design and semiconductor processing technology prepared by non-party semiconductor manufacturing equipment vendors such as Applied Materials, Inc., known as AMAT, and Tokyo Electron Ltd., known as TEL; Plaintiff Micron Technology, Inc.'s Supplemental Opposition to Defendant United Microelectronics Corporation's Motion to Dismiss for Lack of Personal Jurisdiction ("First Micron Opposition"); the Declaration of David Liu, Ph.D. In Support of Micron Technology, Inc.'s Supplemental Opposition to United Microelectronics Corporation's Motion to Dismiss for Lack of Personal Jurisdiction, dated August 12, 2018 ("First Liu Declaration"); Plaintiff Micron Technology, Inc.'s Opposition to Defendant Fujian Jinhua Integrated Circuit Co., Ltd.'s Motion to Dismiss for Insufficient Service of Process and for Lack of Personal Jurisdiction ("Second Micron Opposition"); the Declaration of David Liu, Ph.D. In Support of Micron Technology, Inc.'s Opposition to Fujian Jinhua Integrated Circuit Co. Ltd.'s Motion to Dismiss for Lack of Personal Jurisdiction, dated October 15, 2018 ("Second Liu Declaration"); Plaintiff Micron Technology, Inc.'s Opposition to Defendant United Microelectronics Corporation's Motion to Dismiss Plaintiff's First Amended Complaint ("Third

Micron Opposition"); the Declaration of David Liu, Ph.D. In Support of Plaintiff's Opposition to Defendant United Microelectronics Corporation's Motion to Dismiss Plaintiff's First Amended Complaint, dated March 8, 2019 ("Third Liu Declaration"); and, the following documents cited by and relied on by Dr. Liu in his three declarations, which I will herein refer to collectively as the "Micron/Elpida Process Documents":

- Micron DRAM 90 Series (25nm) Process Traveler ("Micron 90 Series Traveler") (attached to the Clark Decl. as Exhibit 39)
- Micron DRAM 100 Series (20nm) Process Traveler ("Micron 100 Series Traveler") (attached to the Clark Decl. as Exhibit 40)
- Elpida 20nm Process Flow Document ("Elpida Process Document") (attached to the Clark Decl. as Exhibit 41)
- Micron Design Rules for DR25nm ("Micron Design Rules") (attached to the Clark Decl. as Exhibit 42)

The statements in this declaration are made based upon my own personal knowledge, except where otherwise permitted as an expert witness. If called to testify as a witness, I would testify as to the statements and opinions set forth herein.

II. BACKGROUND AND QUALIFICATIONS

2. I am currently an expert consultant in the area of semiconductor design and manufacturing. Since 2010, I have performed this work as a Principal at Berg-Attenborough, Inc., a consulting firm that provides technical consulting and expert witness services to semiconductor companies and law firms. My work as an expert consultant has included developing multi-chip modules that incorporate memory devices such as dynamic random-access memory ("DRAM") and flash memory, as well as performing device analysis and testing using scanning electron microscope ("SEM") technology. In addition to my work as an expert consultant, I have over 35 years of experience as an executive and as an engineer in the semiconductor industry. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980, and I am currently a candidate for a Master of Science degree in Electrical Engineering at the University of California, Berkeley, where I am focusing on analog CMOS circuit design,

simulation, modeling, and processing. A *curriculum vitae* of my educational background and professional experience is attached hereto as Exhibit 1.

III. SUMMARY OF OPINIONS

3. Based upon my study of the First Micron Opposition, the Second Micron Opposition, and the Third Micron Opposition, it is my understanding that Micron has alleged that "UMC … purposefully directed its misconduct at the U.S. by seeking and obtaining patents based on Micron's stolen technology." More specifically, it is my understanding that Micron has alleged that "[s]tarting in September 2016, and publishing in late 2017, UMC and Jinhua have been applying for and obtaining patents based on Micron's trade secrets." It is also my understanding that Micron has further alleged that "[m]any of the UMC/Jinhua Patent Filings describe technologies from Micron's stolen trade secrets …," and that "[g]iven the short period of time from when UMC and Jinhua commenced working on the UMC/Jinhua DRAM Project and the priority dates of the UMC/Jinhua Patent Filings, … Defendants did not and could not have independently developed the DRAM in the UMC/Jinhua Patent filings."

4. Additionally, based upon my study of the First Liu Declaration, the Second Liu Declaration, and the Third Liu Declaration, it is my understanding that Dr. Liu has asserted that "it is highly likely that the disclosures and purported inventions set forth in the [UMC/Jinhua Patents] were derived from or based on Micron's Confidential DRAM Technology ..," and that "it is highly unlikely that UMC/Jinhua independently developed the subject matter described in the [UMC/Jinhua Patents]." It is also my understanding that the only evidence cited by Dr. Liu in support of his opinions is the UMC/Jinhua Patents and the Micron/Elpida Process Documents. It is my understanding that Dr. Liu has not, however, asserted that the UMC/Jinhua patents were "derived from" or "based on" Micron trade secrets, only that they were "derived from" or "based on" "Micron's Confidential DRAM Technology," which Dr. Liu defines as Micron's "confidential information relating to its DRAM devices and processes." Likewise, it is my understanding that Dr. Liu has not asserted that the portions of the Micron/Elpida Process Documents cited in his three declarations constitute Micron trade secrets. A close review of the First Liu Declaration, the

Second Liu Declaration, and the Third Liu Declaration indicates that Dr. Liu never uses the words "trade secret" anywhere in any of his declarations.

5. I have been informed by counsel that a "trade secret" is information that derives "independent economic value" from not being generally known to the public or to other persons who can obtain economic value from its disclosure or use, and that is the subject of reasonable efforts to maintain its secrecy. I have also been informed by counsel that information cannot qualify for trade secret protection if it is "readily ascertainable" by proper means by a person in the industry without significant difficulty, effort, or expense. Furthermore, I have been informed by counsel that information is "readily ascertainable" if it is available in trade journals, reference books, published materials, or commercially available products through reverse engineering. Based upon this understanding of the meaning of a "trade secret," it is my opinion that none of the UMC/Jinhua Patents are "based on," are "derived from," or "describe" any Micron trade secrets.

6. In particular, in my opinion, none of the features identified by Dr. Liu in his three declarations as being both allegedly disclosed in the cited portions of the Micron/Elpida Process Documents, and allegedly "very similar" to the process technology described in the UMC/Jinhua Patents, are entitled to trade secret protection because those features are either generally known to the public, or readily ascertainable by proper means by a person in the industry without significant difficult, effort, or expense. The sources of public information from which these features are "generally known" or "readily ascertainable" include commercially available DRAM products which can be reverse-engineered using techniques that are well-known in the semiconductor industry, completed reverse-engineering reports available from companies such as Chipworks and TechInsights, materials relating to DRAM design and semiconductor processing technology prepared by semiconductor manufacturing equipment vendors such as AMAT and TEL for the benefit of customers who use their equipment, articles from various publications and industry associations, and patents and published patent applications from DRAM manufacturers including not only Micron but also Elpida Memory, Inc. ("Elpida"), Samsung Electronics Co., Ltd. ("Samsung"), Hynix Semiconductor Inc. ("Hynix"), and others.

7. Based upon my analysis of the Micron/Elpida Process Documents, the Micron 90 Series Traveler provides information regarding Micron's 25nm DRAM products (Micron 90 Series Traveler at 1); the Micron 100 Series Traveler provides information regarding Micron's 20nm DRAM products (Micron 100 Series Traveler at 1); the Elpida Process Document provides information regarding Elpida's 25nm DRAM products (Elpida Process Document at 1); and, the Micron Design Rules provide information regarding Micron's 25nm DRAM products (Micron Design Rules at 1). According to information from TechInsights, Micron and Elpida released their 25nm DRAM products at the end of 2013, and they released their 20nm DRAM products at the end of 2014. (TechInsights DRAM Technology/Products Roadmap, August 2018 ("TechInsights 2018 Roadmap"), attached to the Litts Decl. as Exhibit 2, at 2). Therefore, based upon my review of Micron's Complaint, which alleges that UMC developed and set into motion a plan to misappropriate Micron trade secrets sometime in 2015, the semiconductor industry had access to commercially available DRAM products that incorporate the technologies described in the Micron/Elpida Process Documents, including the features identified by Dr. Liu in his three declarations, prior to any alleged wrongdoing in this case. Additionally, the features identified by Dr. Liu are described in numerous patents and published patent applications dating back at least as far as 2009. Furthermore, the features identified by Dr. Liu relating to "double patterning" process steps are described in materials prepared by semiconductor manufacturing equipment vendors and provided to customers who use their equipment.

IV. REVERSE-ENGINEERING

8. Reverse-engineering of competitors' products has become standard practice in the semiconductor industry, including in the DRAM industry, and it provides a remarkable level of detail with respect to the design and manufacture of commercially available semiconductor products. There are two general categories of reverse-engineering for semiconductor devices: circuit extraction and process analysis. (Torrance and James, "Reverse Engineering in the Semiconductor Industry," *IEEE 2007 Custom Integrated Circuits Conference*, pp. 429-436 ("2007 IEEE Paper"), attached as Exhibit 3 to the Litts Decl., at 429). Circuit extraction involves delayering a semiconductor device to obtain samples of the device at each metal and transistor

level; imaging the device using equipment such as a scanning electron microscope ("SEM"); annotating the images by identifying all electronic components, interconnect layers, contacts, and vias; and developing circuit schematics based upon the annotated images. (2007 IEEE Paper at 431-435). The following images show steps in the circuit extraction process:

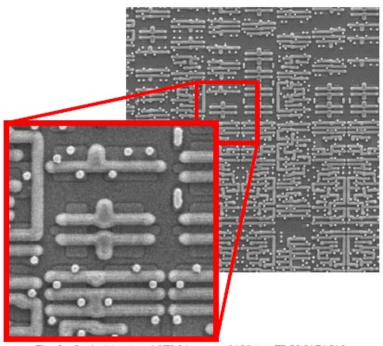


Fig. 8. Optical (top) and SEM images of 130-nm TI OMAP1510

SEM Image

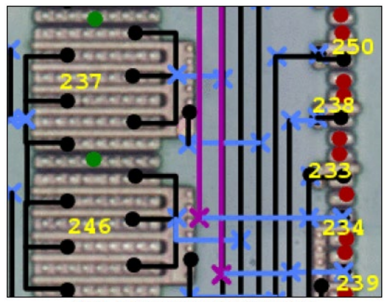
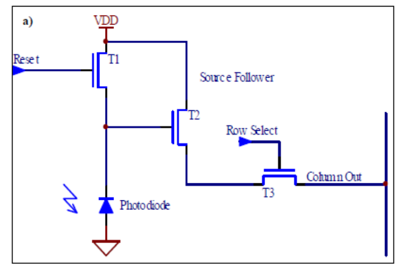


Fig. 10. Image annotated using DAW workstation

Image Annotation



Schematic

(2007 IEEE Pater at 433-434). Process analysis involves obtaining plan-view and cross-sectional images of the device using equipment such as a SEM, a scanning capacitance microscope ("SCM"), or a transmission electron microscope ("TEM"); determining the material composition of the device using techniques such as energy-dispersive x-ray analysis, ion mass spectrometry, or Auger analysis; and determining the layout, structure, and material composition of the device, as well as the process steps used to manufacture the device, based upon the images and material analysis. (2007 IEEE Pater at 434-436). The following are examples of the types of images used in process analysis:

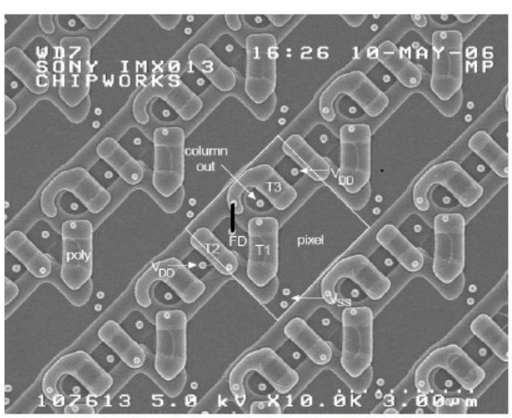


Fig.14. Plan-view SEM of pixels at the polysilicon level

SEM (Plan-view)

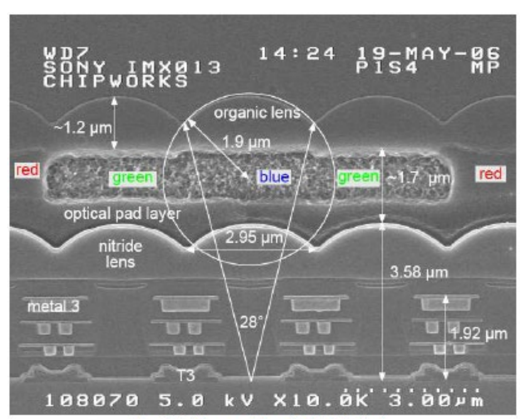


Fig. 15. Cross-sectional SEM of pixels

SEM (Cross-sectional)

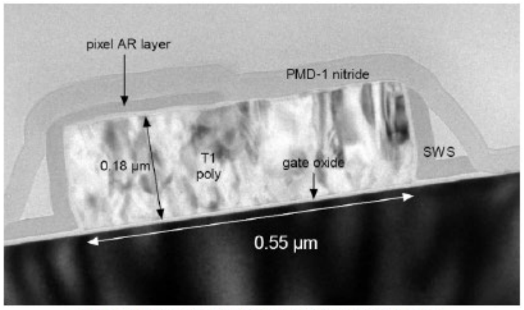


Fig. 16. TEM cross-section of pixel transfer transistor

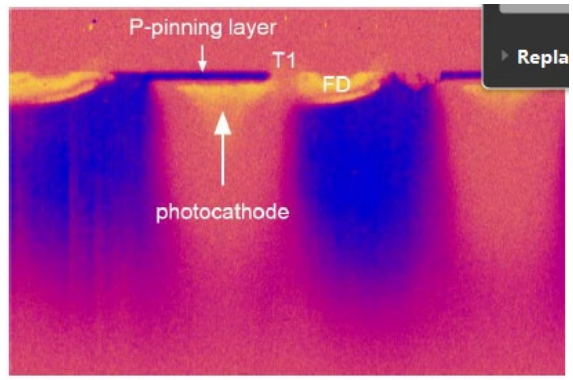


Fig. 17 SCM cross-section of pixels

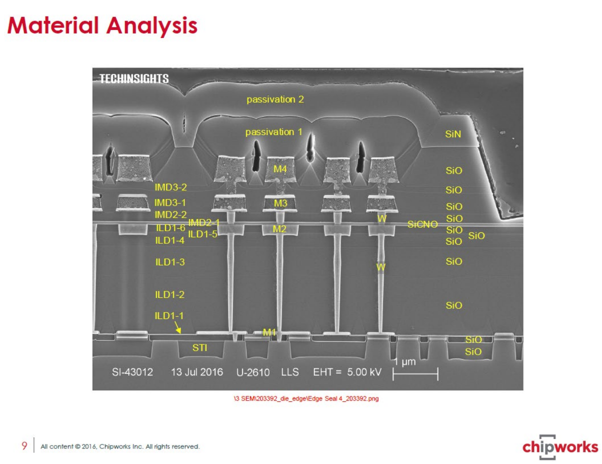
TEM (Cross-sectional) **SCM (Cross-sectional)**

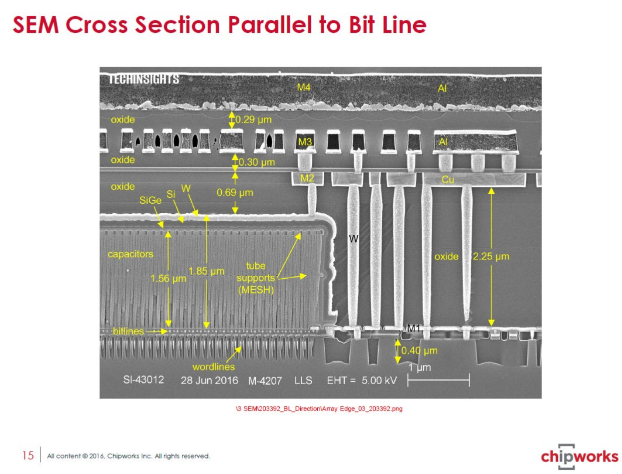
(2007 IEEE Pater at 435-436). Notably, the device layout, structure, material composition, and manufacturing process can be determined through analysis of SEM and TEM images in combination with energy-dispersive x-ray analysis, ion mass spectrometry, or Auger analysis, and the doping structure of features such as transistor source and drain regions and gates can be determined through analysis of SCM images. (2007 IEEE Pater at 435-436). Using a combination of these techniques, the entire layout, structure, and material composition of a DRAM device, and the entire process flow used to manufacture the device, can be determined. (2007 IEEE Pater at 431-436). While this process may seem complicated to those outside of the semiconductor industry, reverse-engineering has become a mandatory practice for all device manufactures, who in the case of DRAM manufacturers typically reverse-engineer a new product from a competitor within a year of its release.

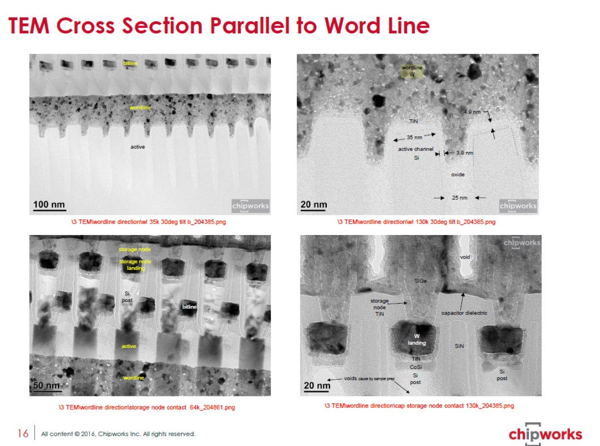
9. The Micron/Elpida Process Documents themselves are replete with SEM and TEM images demonstrating that the information contained therein is readily ascertainable through reverse-engineering. The following examples are taken from the Micron 90 Series Traveler:

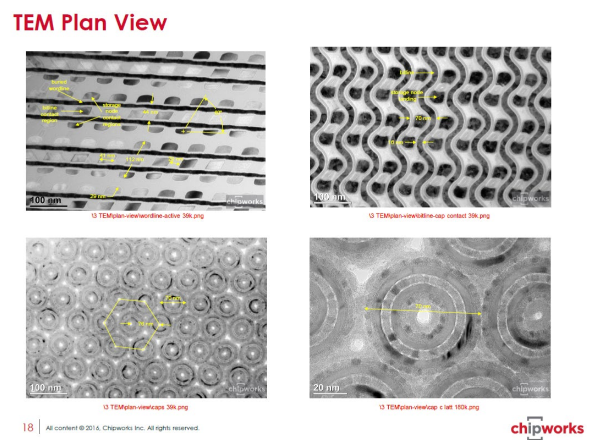
[redacted]

(Micron 90 Series Traveler at pages 9, 14, 32, 67, 106, 136, 168, and 200). Even greater detail is provided in commercial reverse-engineering reports, as demonstrated by the following SEM and TEM images that were included in a Chipworks reverse-engineering report for a commercially available Micron Technology 2y nm GDDR5X SDRAM device:









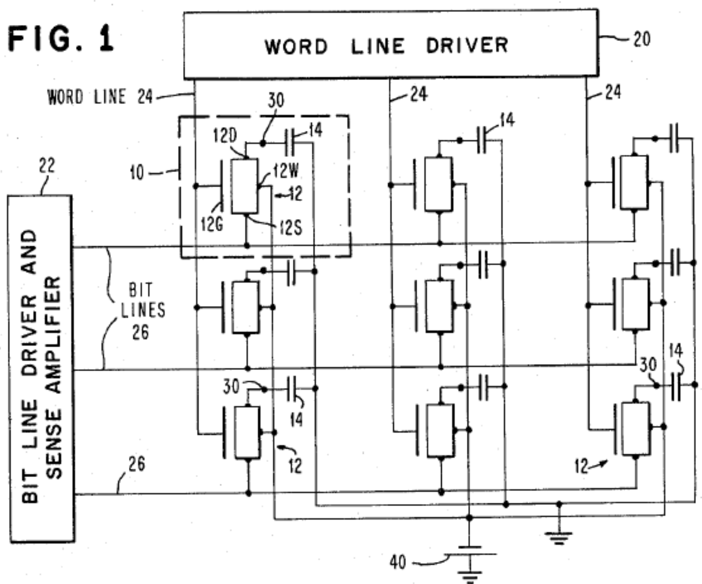
(Chipworks Micron Technology 2y nm GDDR5X SDRAM Process ("Chipworks Micron 2y Report"), attached as Exhibit 4 to the Litts Decl., at 9, 15, 16, and 18). The entire layout, structure, and material composition of Micron's commercially available DRAM products, as well as the process flow for manufacturing those products, can be readily ascertained from this type of commercial reverse-engineering report.

V. PATENTS, PUBLISHED PATENT APPLICATIONS, AND ARTICLES

10. The DRAM technology at issue in this case is generally referred to as one-transistor, one-capacitor (1T1C) DRAM. This technology was invented by Robert H. Dennard, Ph.D. of International Business Machines Corporation ("IBM") and patented in U.S. Patent No.

3,387,286 ("'286 1T1C Patent") (attached as Exhibit 5 to the Litts Decl.), which was filed on July 14, 1967 and issued on June 4, 1968. The revolutionary advancement of the '286 1T1C Patent was the use of memory cells 10 comprising a single transistor 12 and a single capacitor 14, as shown in Fig. 1 of the patent:

FIG. 1



Read and write operations are performed in cycles and are controlled by word line drivers 20, and by bit line drivers and sense amplifiers 22. ('286 1T1C Patent at 4:1-5). The word line drivers 20 are connected to the gates 12G of the transistors 12 in the memory cells 10 by word lines 24 ('286 1T1C Patent at 4:48-52), the bit line drivers and sense amplifiers 22 are connected to the source terminals 12S of the transistors 12 by bit lines 26 ('286 1T1C Patent at 4:56-61), and the capacitors 14 which store information are connected to the drain terminals 12D of the transistors 12 ('286 1T1C Patent at 3:44-48). Read operations involve applying signals from the word line driver 20 to the transistor gates 12G via the appropriate word line 24, causing signals representative of stored information to be transmitted from the capacitors 14 to the bit line driver and sense amplifier 22 via the bit lines 26. ('286 1T1C Patent at 4:48-73). Write operations, which immediately follow read operations, involve applying signals from the bit line driver and sense amplifier 22, with the signal from the word line driver 20 still being applied to the transistor gates 12G via the word lines 24, causing either the same information or new information to be stored in the capacitors 14. ('286 1T1C Patent at 4:74-5:24). After a read-write cycle, the signal applied to a particular transistor

gate 12G by the word line driver 20 via a word line 24 is terminated, thus causing a charge (or lack of charge) representing binary information to be stored in the capacitor 14 until the next read-write cycle for that particular memory cell 10. ('286 1T1C Patent at 5:24-30). This same circuit design has been used in virtually every commercial DRAM device ever manufactured since the invention of the technology more than fifty years ago.

11. While the circuit design and method of operation of DRAM devices has not changed since the technology was invented in the 1960s, its layout, structure, and material composition has evolved since that time. Modern DRAM devices, including those at issue in this case, are generally referred to capacitor-over-bitline ("COB") DRAM because, as the name implies, the capacitor is located above the bitlines, with contact between the transistor drain terminals and the capacitors being made by storage node contacts that extend upwards from the transistors to the capacitors between the wordlines and the bitlines, as is shown in the following top view of COB memory cells from an article published in the IEEE Journal of Solid-State Circuits in 2001:

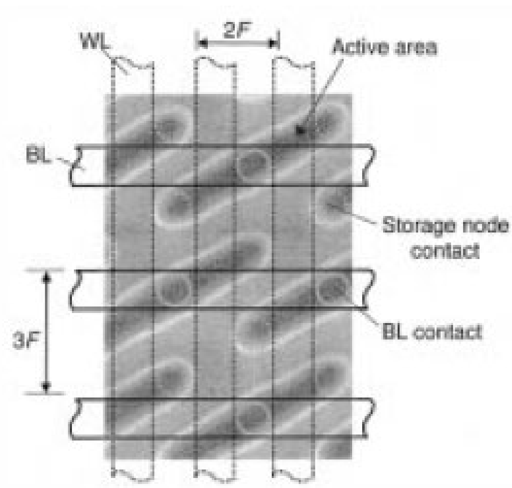


Fig. 2. $6F^2$ cell.

(Takahashi *et al.*, "A Multigigabit DRAM Technology With 6F2 Open-Bitline Cell, Distributed Overdriven Sensing, and Stacked-Flash Fuse," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 11, November 2001, pp. 1721-1727 ("2001 IEEE Paper"), attached as Exhibit 6 to the Litts Decl., at 1722). As can be seen in this image, each "active area" is intersected by one bitline and by two wordlines, thus creating two transistors per active area that share a single source terminal

(connected to a bitline via a bitline contact) but that have separate drain terminals (each connected to a capacitor via a storage node contact), with the wordlines functioning as the gates of the transistors. (2001 IEEE Paper at 1722). The following schematic illustrations and cross-sectional images of a Samsung 90nm DRAM device having this structure are from a conference paper published by Chipworks in 2010:

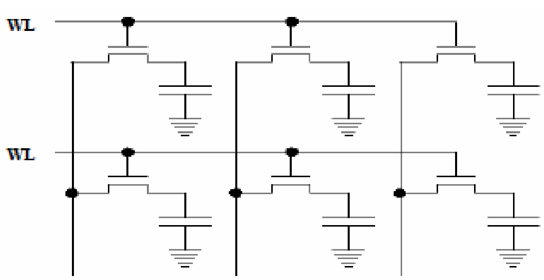


Fig. 1. Schematic of 2 x 3 1T-1C DRAM Cell Block

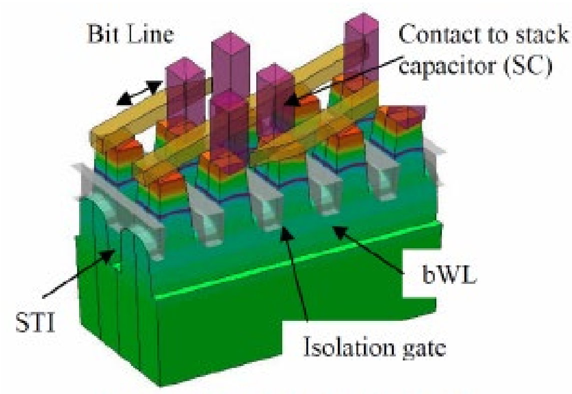


Fig. 13. Schematic of Buried Wordline Cell [4]

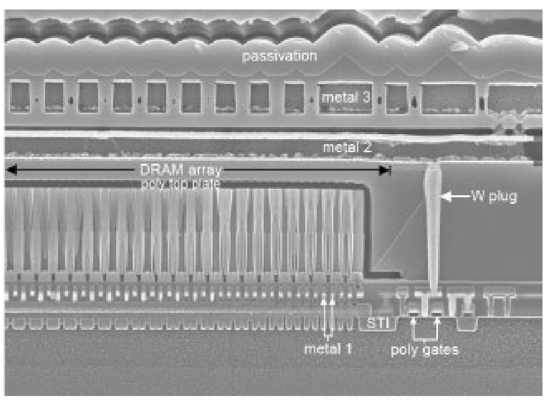


Fig. 2. Cross-Section of Samsung 90-nm 512 Mb SDRAM

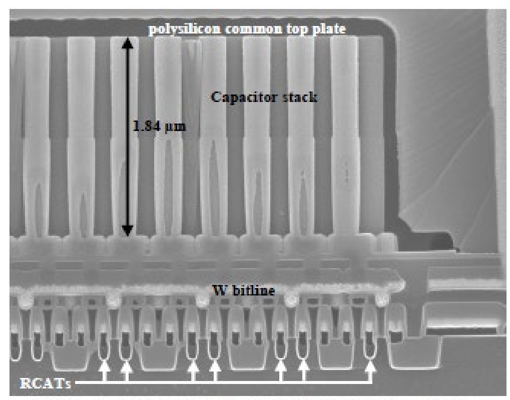


Fig. 3. Close-up of Cell Array in Samsung 90-nm 512 Mb SDRAM

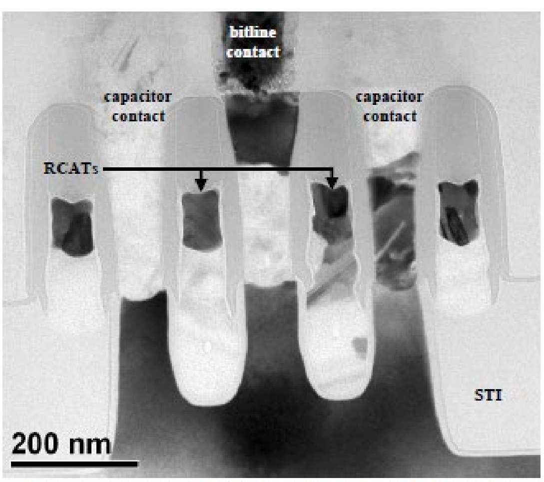


Fig. 4. Recess-Channel-Array Transistors in Samsung 90-nm 512 Mb SDRAM

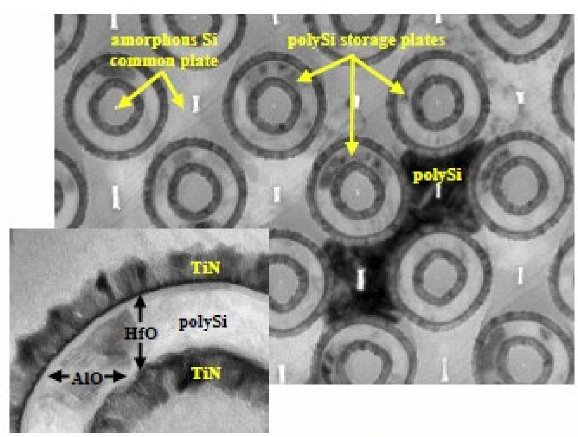


Fig. 5. Planar Section of Capacitors in Samsung 90-nm 512 Mb SDRAM

(James, "Recent Innovations in DRAM Manufacturing," *IEEE Xplore*, August 2010 ("2010 IEEE Paper"), attached as Exhibit 7 to the Litts Decl.). The 2001 IEEE Paper and the 2010 IEEE Paper describe the same layout and structure incorporated in the DRAM technology at issue in this case.

12. The technology at issue in this case is also disclosed in numerous United States and foreign patents and published patent applications dating back more than twenty-five years. The earliest patent of which I am aware that discloses the exact cell layout depicted in the Micron/Elpida Process Documents is U.S. Patent No. 5,398,205 ("'205 Patent") (attached as Exhibit 8 to the Litts Decl.), which was filed by NEC Corporation on May 9, 1994, claiming priority to a Japanese patent application that was filed on May 10, 1993, and which issued on March 14, 1995. The '205 Patent discloses a DRAM device having a plurality of cell active regions 1, each being surrounded by a trench isolation region 7 comprising a trench 7-1 formed in a silicon substrate 10 and an insulating material 7-2 such as silicon dioxide, as is shown in Figs. 2 and 3 of the patent:

FIG. 2

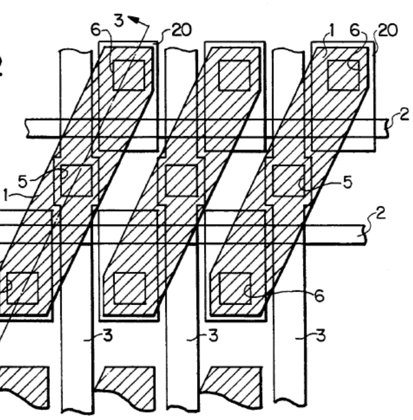
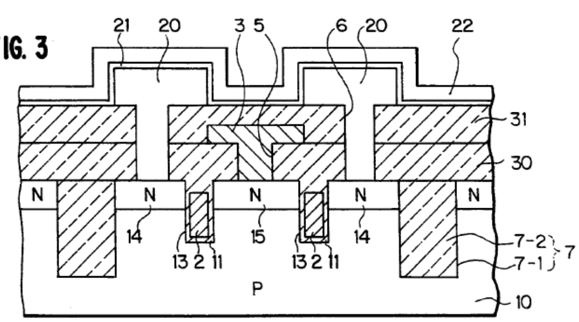


FIG. 3



('205 Patent at 2:30-42). Two word lines 2 cross each cell active region 1 so as to form two memory cells in each cell active region 1, each word line 2 being formed in a trench 13 and acting as a gate electrode of one memory cell transistor. ('205 Patent at 2:45-3:4). Trenches 13 have a smaller depth than trenches 7 that surround the cell active regions 1, and each trench 13 is covered with a gate insulating film 11 that isolates the word lines 2 from the substrate 10. ('205 Patent at 2:54-64). An insulating layer 30 covers the top surface of the word lines 2 and the substrate 10, and a plurality of bit line contact holes 5 are provided in the insulating layer 30 to expose the drain regions 15 of the memory cell transistors. ('205 Patent at 2:64-68, 3:5-9). Bit lines 3 are connected

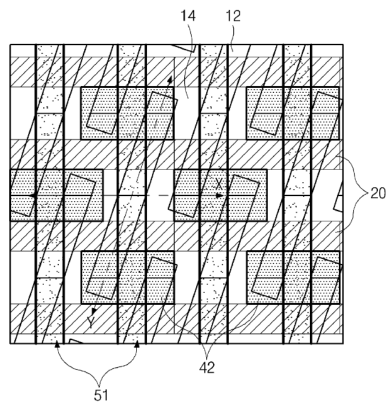
to the exposed drain regions 15 through the contact holes 5, and an insulating layer 31 such as silicon oxide is formed to cover the insulating layer 30 and the bit lines 3. ('205 Patent at 2:64-68, 3:9-15). Capacitor contact holes 6 are provided in the insulating layers 30 and 31 to expose the source regions 14 of the memory cell transistors, and a storage electrode 20 is formed through the capacitor contact holes 6. ('205 Patent at 2:64-68, 3:16-22). Finally, a dielectric film 21 is formed over the entire surface of each storage electrode 20 and the insulating layer 31, and a polysilicon cell plate electrode 22 is formed on the dielectric film, thus forming memory cell capacitors that are connected to the memory cell transistor source regions 14. ('205 Patent at 2:64-68, 3:22-27).

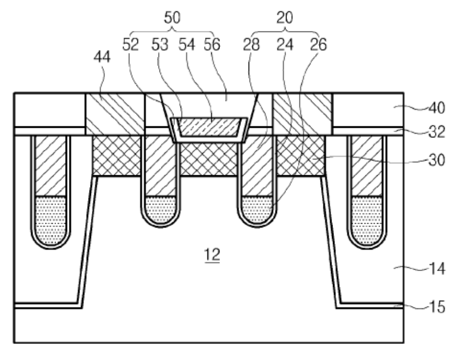
13. For purposes of comparison, the following images from the Micron 90 Series Traveler show that the technology disclosed therein is virtually identical to that disclosed in the '205 Patent:

[redacted]

Furthermore, this same technology is depicted in numerous other patents and published patent applications that predate any alleged wrongdoing in this case, including:

- U.S. Patent No. 8,048,737 ("'737 Patent") (attached as Exhibit 9 to the Litts Decl.), which was filed by Hynix on December 29, 2009, claiming priority to a Korean patent application that was filed on August 11, 1009, and which issued on November 1, 2011:





(a)

- U.S. Published Patent App. No. 2007/0023784 ("'784 Publication") (attached as Exhibit 10 to the Litts Decl.), which was filed on July 26, 2006, claiming priority to a German patent application that was filed on July 29, 2005, and which was published on February 1, 2007:

FIG 2D

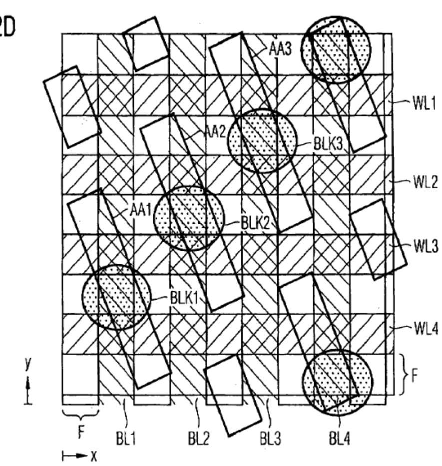
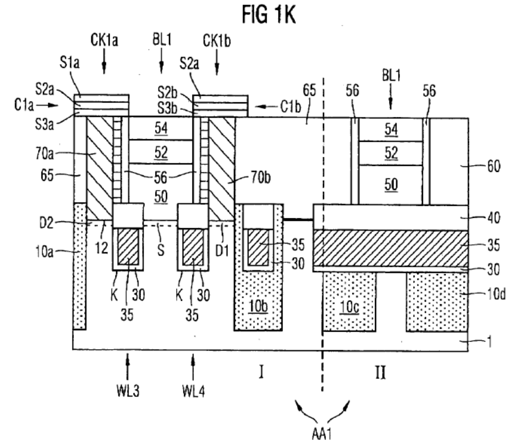


FIG 1K



- U.S. Published Patent App. No. 2008/0283957 ("'597 Publication") (attached as Exhibit 11 to the Litts Decl.), which was filed by Samsung on April 30, 2008, claiming priority to a Korean patent application that was filed on May 18, 2007, and which was published on November 20, 2008:

FIG. 10

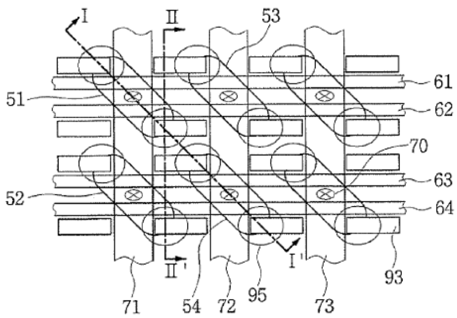
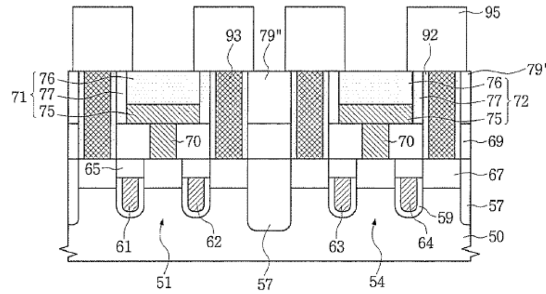


FIG. 13A



- U.S. Published Patent App. No. 2010/0200948 ("'948 Publication") (attached as Exhibit 12 to the Litts Decl.), which was filed by Hynix on June 26, 2009, claiming priority to a Korean patent application that was filed on February 10, 2009, and which was published on August 12, 2010:

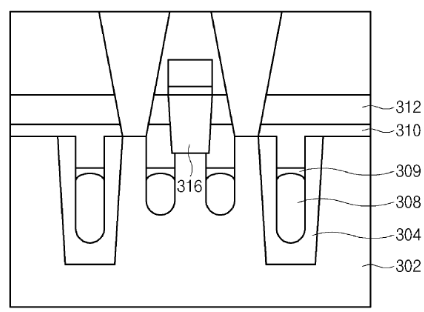


Fig.3

- U.S. Published Patent App. No. 2010/0270602 ("'602 Publication") (attached as Exhibit 13 to the Litts Decl.), which was filed by Hynix on June 29, 2009, claiming priority to a Korean patent application that was filed on April 24, 2009, and which was published on October 20, 2010:

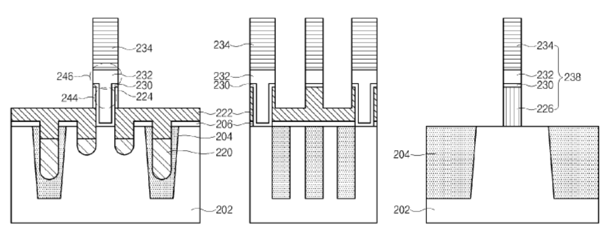


Fig.2o

- U.S. Published Patent App. No. 2010/02327407 ("'407 Publication") (attached as Exhibit 14 to the Litts Decl.), which was filed by Hynix on November 9, 2009, claiming priority to a Korean patent application that was filed on June 29, 2009, and which was published on December 30, 2010:

FIG. 16

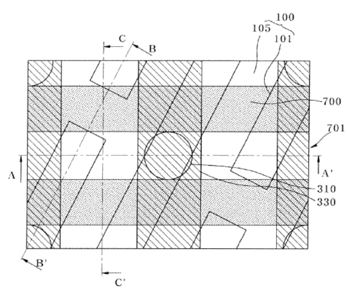
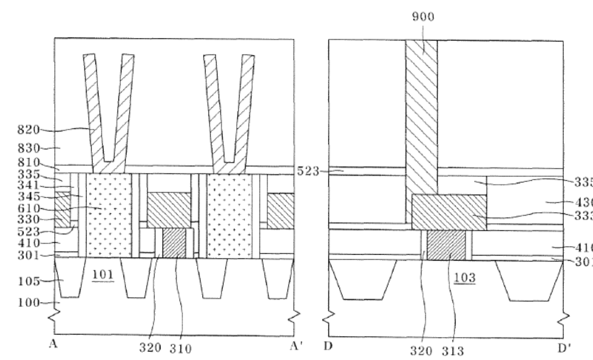


FIG. 21



- U.S. Published Patent App. No. 2012/0132971 ("'271 Publication") (attached as Exhibit 15 to the Litts Decl.), which was filed by Elpida on November 30, 2011, claiming priority to a Japanese patent application that was filed on November 30, 2010, and which was published on May 31, 2012:

FIG. 1

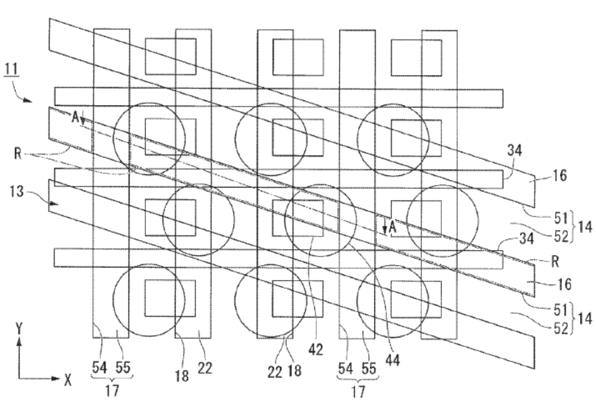
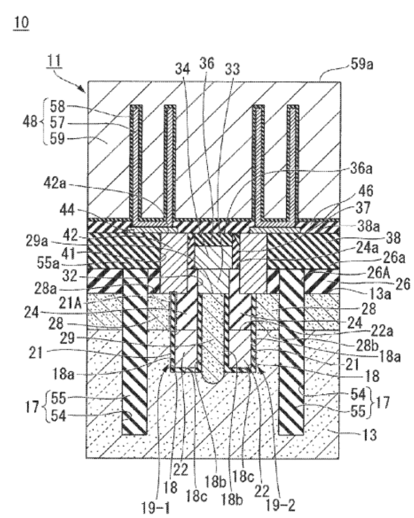


FIG. 2



- U.S. Published Patent App. No. 2012/0264298 ("'298 Publication") (attached as Exhibit 16 to the Litts Decl.), which was filed by Hynix on June 12, 2012, claiming priority to a Korean patent application that was filed on April 19, 2010, and which was published on October 18, 2012:

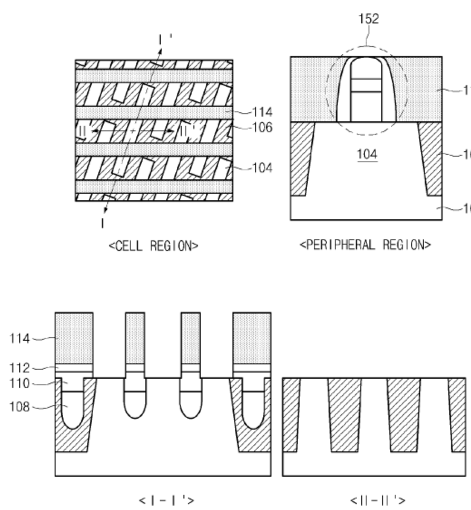


Fig.1

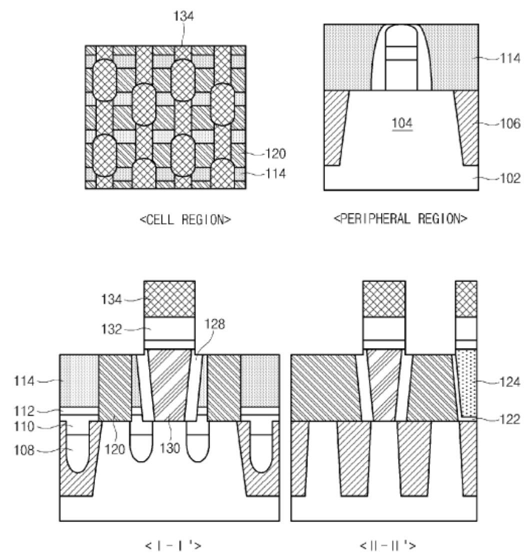


Fig.7

- U.S. Published Patent App. No. 2013/0015551 ("'551 Publication") (attached as Exhibit 17 to the Litts Decl.), which was filed on July 14, 2011, and which was published on January 17, 2013:

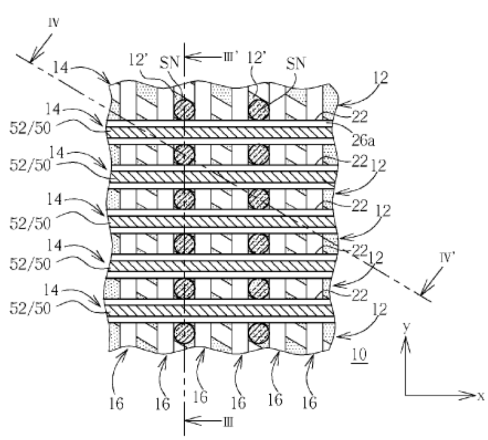


FIG. 6A

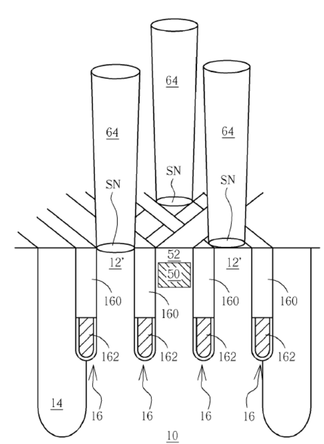


FIG. 7

- U.S. Published Patent App. No. 2014/0264517 ("'517 Publication") (attached as Exhibit 18 to the Litts Decl.), which was filed by Samsung on February 7, 2014, claiming priority to a Korean patent application that was filed on March 15, 2013, and which was published on September 18, 2014:

Fig. 2

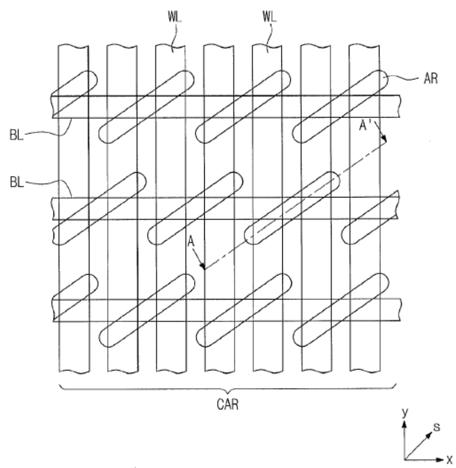
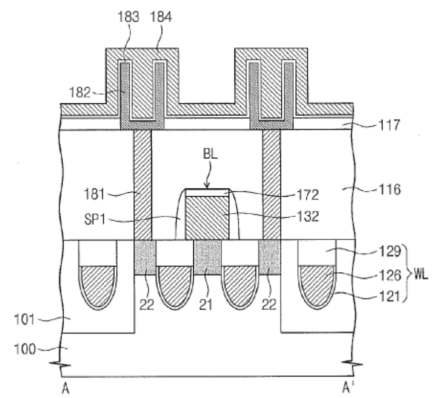


Fig. 9A



Each of these patents and published patent applications discloses the same memory cell structure as described in the Micron/Elpida Process Documents.

VI. MATERIALS FROM SEMICONDUCTOR MANUFACTURING EQUIPMENT VENDORS

14. The manufacture of a semiconductor device, also called device fabrication, involves performing a sequence of photolithographic and chemical processing steps which, collectively, are referred to as the process flow for the device. These processing steps typically include one or more of the following:

- Wet cleaning;
- Thin film deposition (*e.g.*, physical vapor deposition ("PVD"), chemical vapor deposition ("CVD"), electrochemical deposition ("ECD"), atomic layer deposition ("ALD"), etc.);
- Removal (*e.g.*, etching, chemical mechanical planarization ("CMP"), etc.);
- Patterning (*e.g.*, lithography, double patterning, etc.); and
- Electrical properties modification (*e.g.*, ion implantation, annealing, oxidation, etc.).

The equipment that is used by a wafer fab such as UMC to perform these processing steps is manufactured by companies such as AMAT and TEL. These companies typically develop best-known methods ("BKMs") for performing processing steps using their equipment. These BKMs typically include detailed instructions, often with schematics, along with process parameters for performing the required steps.

15. It is commonplace in the industry for semiconductor manufacturing equipment vendors to provide BKMs as well as additional guidance to their customers with respect to using their equipment to manufacture a desired structure. For example, the following documents from AMAT provide guidance with respect to performing double patterning using their equipment:

[redacted]

[redacted]

[redacted]

(UMC-TEL Etch DRAM Status Update, Jun 13th, 2016 ("[redacted]"), attached as Exhibit 20 to the Litts Decl., at 1, 5, 9, 10, 11, and 12). BKMs such as these examples from AMAT and TEL would be available for other processing steps performed using these companies' equipment, and they would be far more useful to a fab such as UMC than information contained in a competitor's process documents, which would almost certainly be tuned for different equipment.

VII. ANALYSIS OF UMC/JINHUA PATENTS AND PURPORTED MICRON CONFIDENTIAL DRAM TECHNOLOGY

A. The '901 Patent

17. The '901 Patent generally discloses and claims increasing the width of the edges of the ends of the active areas at the boundary of the device region. ('901 Patent at 1:50-95). This active area structure helps prevent tipping of the films adjacent the boundary of the device region typically caused by thermal stress generated by film deposition, or by film stress due to differences in pattern density between the device and the peripheral region. ('901 Patent at 2:44-52). Various embodiments of active areas formed in accordance with the invention of the '901 Patent are shown in Figs. 1B, 2B, and 3:

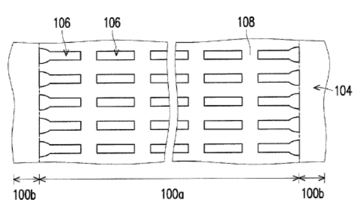


FIG. 1B

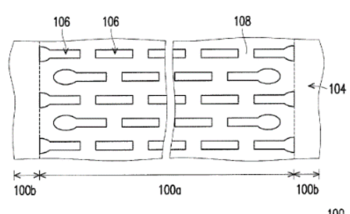


FIG. 2B

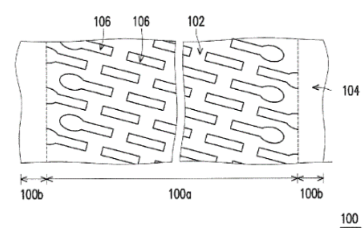


FIG. 3

In my opinion, the '901 Patent is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

18. Dr. Liu states with respect to the '901 Patent that "[redacted]" In support of this statement, Dr. Liu cites to page 12 of the Micron 90 Series Traveler, and to page 16 of the Micron 100 Series Traveler. Contrary to Dr. Liu's statement, however, these pages of Micron's process travelers do not disclose these features. In particular, the cited pages of

these documents include [redacted]:

[redacted]

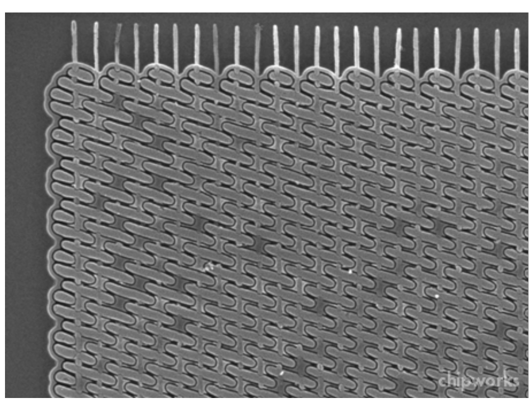
Even if Micron's devices included the features identified by Dr. Liu, there would be no way to see these features in these schematic drawings because they do not provide the requisite level of detail. There is simply no way to determine from these drawings, or from any other information provided on the cited pages of Micron's process travelers, the [redacted].

19. Dr. Liu also cites to Figs. 2-1 and 12-1 of the Micron Design Rules in support of his statement that [redacted]":

[redacted]

Contrary to Dr. Liu's assertions, however, these figures of the Micron Design Rules show that the [redacted]. Moreover, while the concept of dummy structures is not mentioned anywhere in the '901 Patent, Figs. 2-1 and 12-1 of the Micron Design Rules do not indicate the presence of a "[redacted]" contrary to Dr. Liu's assertions.

20. Furthermore, even if Micron's process travelers and design rules showed the features identified by Dr. Liu, these features would not, in my opinion, constitute trade secrets because they would have been readily ascertainable by proper means by a person in the industry. Specifically, the [redacted] is clearly visible in a plan-view SEM image of the active area of a device, such as the following SEM image of the active areas of a Samsung 2Gb DDR3 SDRAM device:



("Samsung's 3x DDR3 SDRAM – 4F2 or 6F2? You Be the Judge..," Solid State Technology, January 31, 2011 ("2011 Solid State Paper"), attached as Exhibit 21 to the Litts Decl., at 3). As can be seen in this SEM image, any variation in the widths of the active areas of the device would be clearly shown. SEM images such as this are available from vendors such as TechInsights and Chipworks, and many such images (such as this one) are freely available for download on the World Wide Web.

21. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '901 Patent were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '901 Patent describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

B. The '790 Patent and the '167 Patent

22. The '790 Patent generally discloses and claims providing a landing pad in second connecting structures located beneath the storage nodes of a DRAM device but excluding the landing pad from first connecting structures located beneath dummy nodes. ('790 Patent at 6:48-58). By excluding the landing pad from the first connecting structures beneath the dummy nodes, more dummy nodes can be formed per unit area to increase pattern density in the memory region, thus eliminating or reducing the problems associated with differences in pattern density between the memory region and the peripheral region, resulting in improved performance when the DRAM device is further integrated and miniaturized. ('790 Patent at 6:48-65). First and second

conductive structures formed beneath dummy nodes and storage nodes, respectively, in accordance with the invention of the ’790 Patent are shown in Figs. 4 and 5:

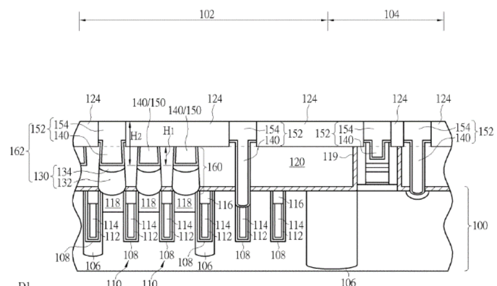


FIG. 4

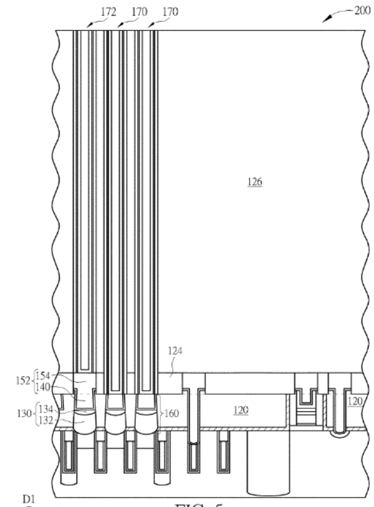


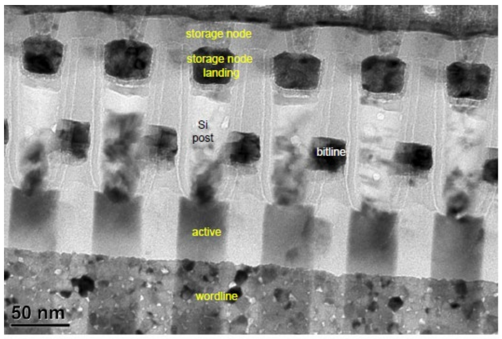
FIG. 5

The ’167 Patent, which has the same specification as the ’790 Patent, claims a method for forming the semiconductor device claimed in the ‘790 Patent. In my opinion, neither the ’790 Patent nor the ’167 Patent is “based on,” is “derived from,” or “describes” any Micron trade secrets.

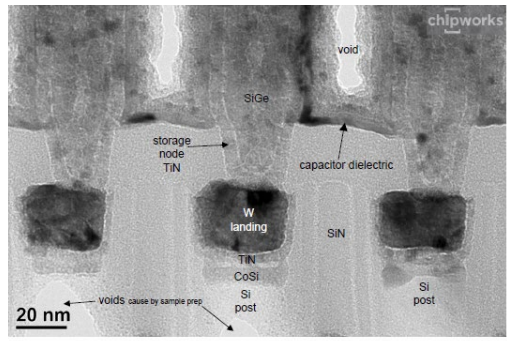
23. Dr. Liu states with respect to the ’790 Patent that “[redacted]” In support of this statement, Dr. Liu cites to page 179 of the Micron 90 Series Traveler, and to page 211 of the Micron 100 Series Traveler. Micron’s own process documents, however, show that these features are readily ascertainable by proper means through reverse-engineering. They do so by providing transmission electron microscopy (“TEM”) images of Micron devices:

[redacted]

Moreover, the identification of these features as well as the material composition of those features is likewise readily ascertainable through reverse-engineering, as can be seen in the following TEM image analysis prepared by Chipworks for a commercially available Micron Technology 2y nm GDDR5X SDRAM device:



\3 TEM\wordline direction\storage node contact 64k_204861.png



\3 TEM\wordline direction\cap storage node contact 130k_204385.png

(Chipworks Micron 2y Report at 16). Therefore, in my opinion the features identified by Dr. Liu are not trade secrets because they would be readily ascertainable from reverse-engineering of commercially available DRAM products.

24. Dr. Liu also states that "[redacted]. In

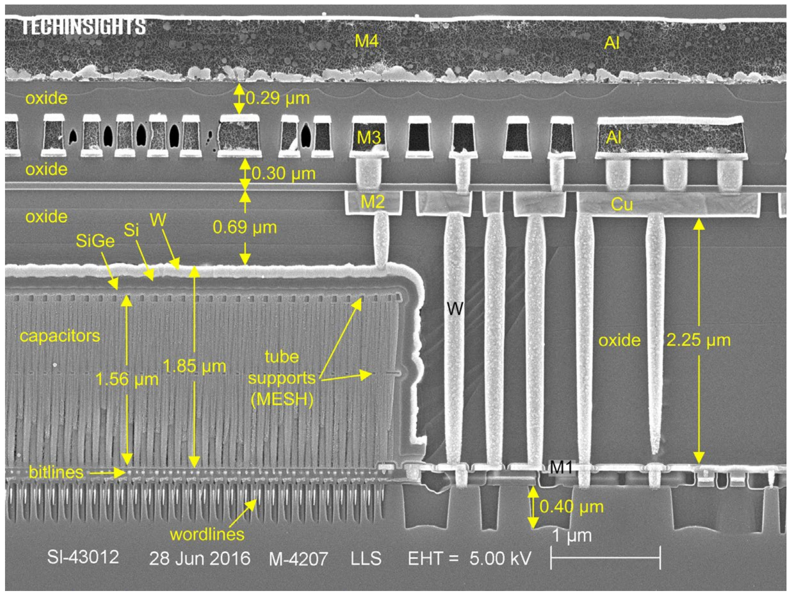
support of these statements, Dr. Liu cites to page 201 of the Micron 90 Series Traveler, and to page 243 of the Micron 100 Series Traveler, which include the following figures:

[redacted]

Again, however, Micron's own process documents show that these features are readily ascertainable by proper means through reverse-engineering by providing either SEM or TEM images of Micron devices:

[redacted]

Even more detail is shown in reverse-engineering analysis provided by third parties, such as the following SEM image prepared by Chipworks for a commercially available Micron Technology 2y nm GDDR5X SDRAM device:



(Chipworks Micron 2y Report at 15). Therefore, in my opinion the features identified by Dr. Liu in connection with the ’790 Patent are not trade secrets because they would be readily ascertainable from reverse-engineering of commercially available DRAM products.

25. For these reasons, I disagree with Dr. Liu’s opinion that “it is highly likely that the disclosures and purported inventions set forth in the ’790 Patent were derived from or based on Micron’s Confidential DRAM Technology …,” as well as his opinion that “[t]he ’790 Patent describes the same or very similar process technology as described in Micron’s Confidential DRAM Technology that I understand was in UMC’s possession.” For the same reasons, I disagree with Dr. Liu’s opinions with respect to the ’167 Patent.

C. The '283 Patent

26. The '283 Patent generally discloses and claims a semiconductor memory structure and method of fabrication in which the gate structure in the peripheral circuit region is formed before the bit lines in the memory cell region and the dummy bit line in the cell edge region, thereby simplifying the fabrication process. ('283 Patent at 5:54-64). Additionally, the bit lines and the dummy bit line are formed with improved precision by using a sidewall image transfer ("SIT") process (also called a self-aligned double patterning ("SADP") process), resulting in improved process yield. ('283 Patent at 4:52-59, 7:26-33). Specifically, the '283 Patent teaches forming a dummy bit line in the cell edge region of a semiconductor device (between the memory cell region and the peripheral region) that comprises an outer line portion and a first inner line portion having different widths from one another, extending along a first direction D1, and collectively overlapping at least two active regions along a second direction D2 (that is perpendicular to the first direction D1), as shown in Figs. 7A and 7B:

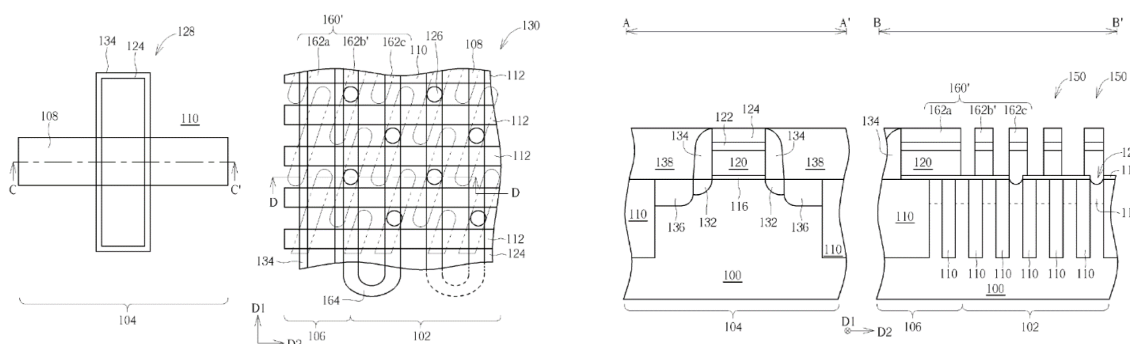


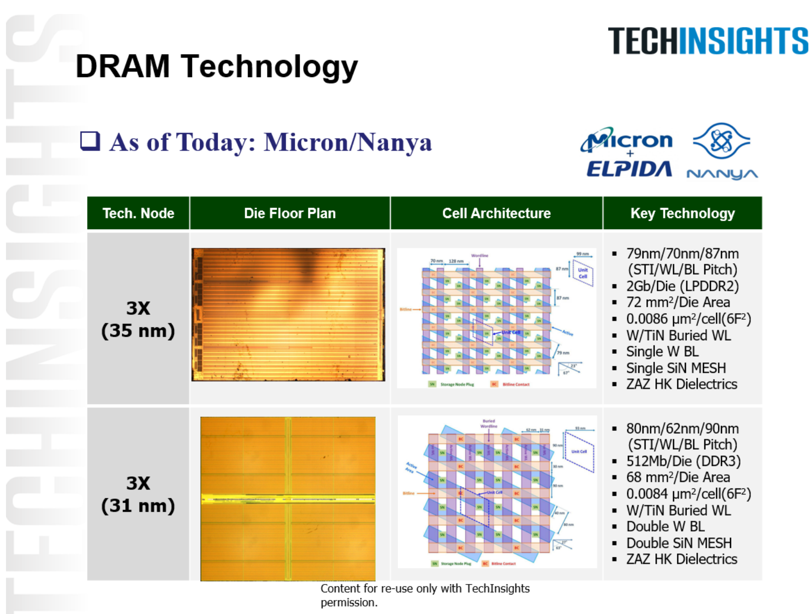
FIG. 7A FIG. 7B

('283 Patent at 5:34-54). Optionally, the dummy bit line may also include a second inner line portion that likewise extends along the first direction D1. ('283 Patent at 6:22-53). Additionally, a plurality of bit lines may be formed in the memory cell region, and a gate structure may be formed in the peripheral circuit region. ('283 Patent at 5:34-64). In my opinion, the '283 Patent is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

27. Dr. Liu states with respect to the ’283 Patent that “[redacted]” citing pages 10 and 104 of the Micron 90 Series Traveler, as well as pages 10 and 127 of the Micron 100 Series Traveler, as support. These pages include schematic layouts of the active regions, bitlines, and wordlines in Micron’s devices:

[redacted]

The schematic layouts shown in Micron’s process travelers are remarkably similar to those available from reverse-engineering reports from TechInsights:



(TechInsights DRAM Technology/Products Roadmap, October 2014 ("TechInsights 2014 Roadmap"), attached to the Litts Decl. as Exhibit 22, at 7). Moreover, nearly every modern DRAM device includes "[redacted]" including devices from not only Micron but also its primary competitors, including Samsung:

[redacted]

(Chipworks Micron 2y Report at 17). In fact, this the exact same memory cell design that is shown in the '205 Patent, which was filed by NEC Corporation on May 9, 1994, claiming priority to a Japanese patent application that was filed on May 10, 1993, and which issued on March 14, 1995:

FIG. 2

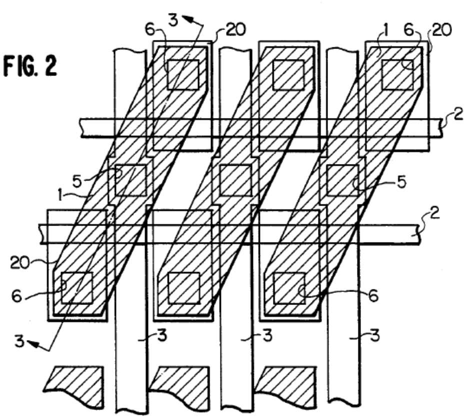
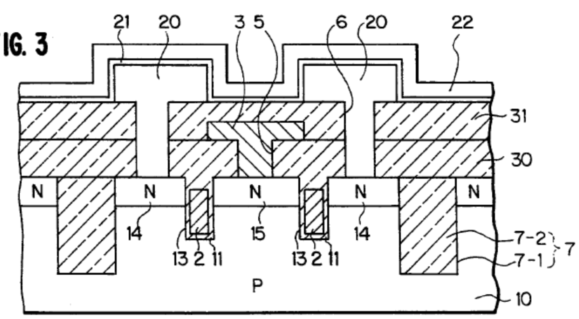
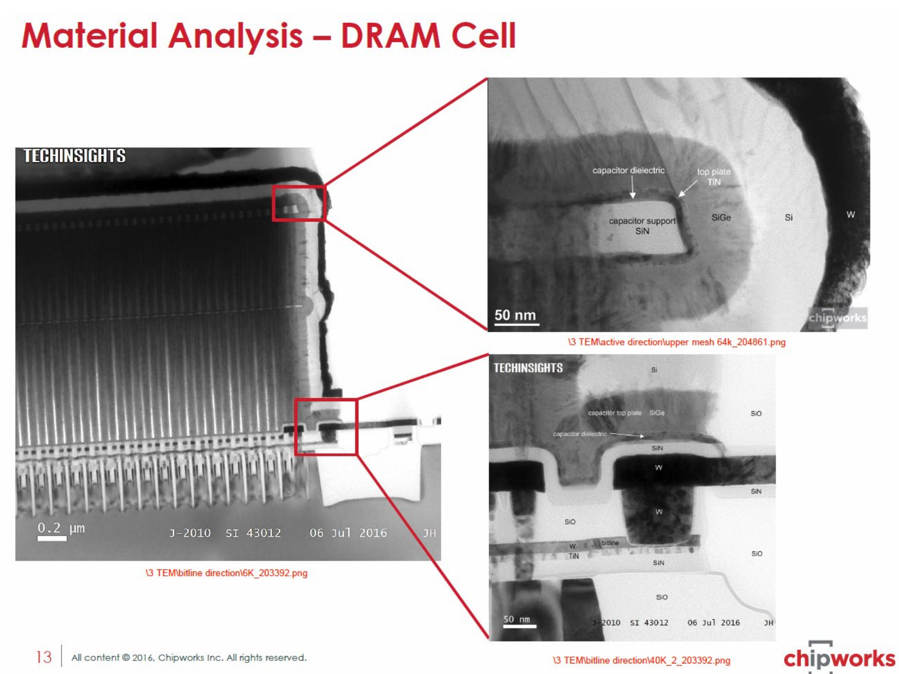


FIG. 3



This DRAM cell design is readily ascertainable from reverse-engineering of commercially available DRAM products, and it has been well known in the DRAM industry for more than twenty years.

28. Dr. Liu also states that "[redacted]" this time citing pages 8 and 104 of the Micron 90 Series Traveler, pages 10 and 127 of the Micron 100 Series Traveler, and page 55 of the Elpida Process document as support. Similarly, Dr. Liu asserts that "[redacted]" citing Fig. 12-2. These pages, however, either do not provide the requisite level of detail, or simply just fail, to show the structure – or even the presence – of any [redacted]. If Micron's devices did [redacted] however, these structures would be clearly visible in SEM or TEM images obtained through reverse-engineering, such as the following TEM images prepared by Chipworks for a commercially available Micron Technology 2y nm GDDR5X SDRAM device:



(Chipworks Micron 2y Report at 14). Therefore, in my opinion the features identified by Dr. Liu in connection with the '283 Patent are not trade secrets because they would be readily ascertainable from reverse-engineering of commercially available DRAM products.

29. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '283 Patent were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '283 Patent describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

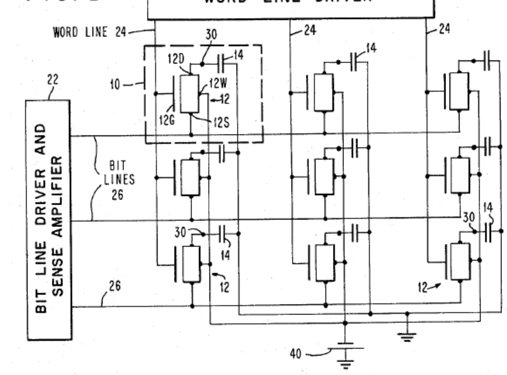
D. The '162 Patent

30. The '162 Patent generally discloses and claims a method of fabricating a semiconductor device that avoids the damage to the spacers and capping layers surrounding the bit lines that could occur when forming the storage node contact plugs using prior techniques. ('162 Patent at 5:5-29). Specifically, the claimed method involves forming storage node contact plugs within apertures defined by essentially homogenous dielectric sidewalls of an isolation mesh that physically separates and electrically isolates the storage node contact plugs from the bit line contact plugs and bit lines. ('162 Patent at 8:15-59). The claimed isolation mesh is formed of the same insulation material used to form the spacers and capping layers surrounding the bit lines, using a sequence of processes that repairs any damage that may have occurred to spacers and capping layers prior to forming the apertures within which the storage node contact plugs are formed. ('162 Patent at 7:66-8:14). In my opinion, the '162 Patent is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

31. Dr. Liu states with respect to the '162 Patent that "[redacted]" citing pages 145-160 of the Micron 90 Series Traveler, and pages 184-195 of the Micron 100 Series Traveler. This is a fundamental

feature of the 1T1C DRAM circuit invented by Dr. Dennard in 1967, as shown in Fig. 1 of his '286 1T1C Patent:

FIG. 1



This feature has been incorporated in possibly every commercial DRAM device ever manufactured, including the '205 Patent, which was filed by NEC Corporation on May 9, 1994, claiming priority to a Japanese patent application that was filed on May 10, 1993, and which issued on March 14, 1995:

FIG. 2

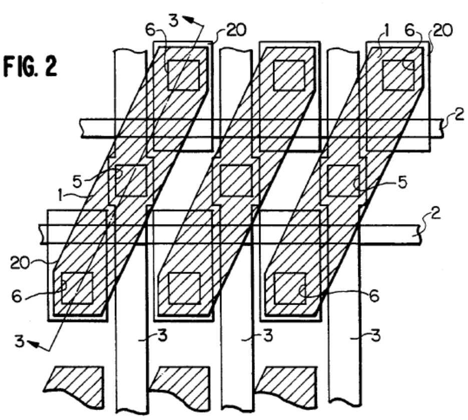
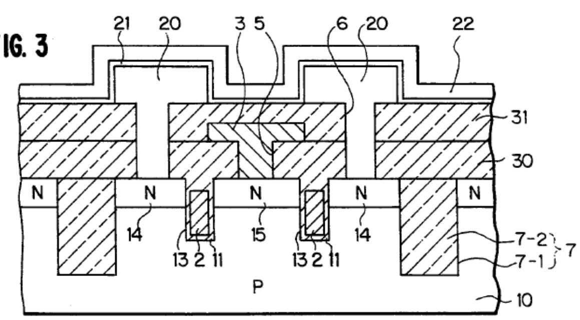
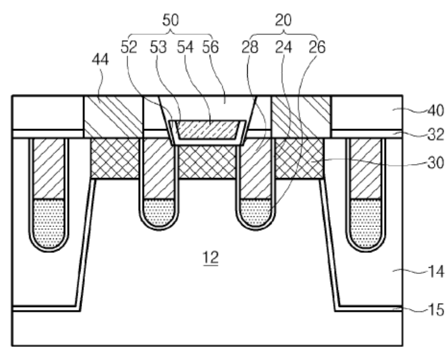


FIG. 3



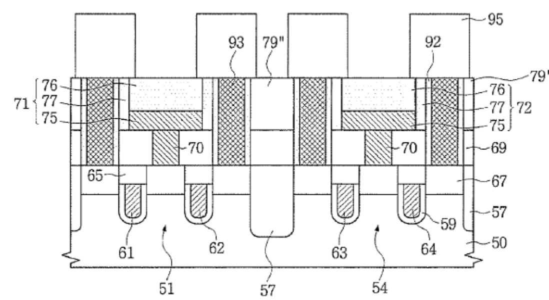
32. Dr. Liu also states that "[redacted]" citing page 159 of the Micron 90 Series Traveler, and page 194 of the Micron 100 Series Traveler, as support. This is a fundamental feature of COB DRAM, in which the [redacted], and is shown in numerous patents disclosing this type of DRAM, including the following:



(a)

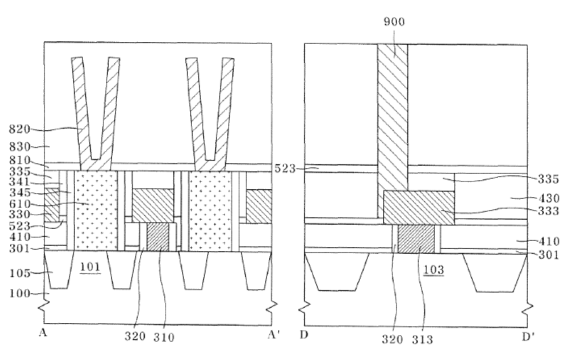
'737 Patent (issued 2011)

FIG. 13A



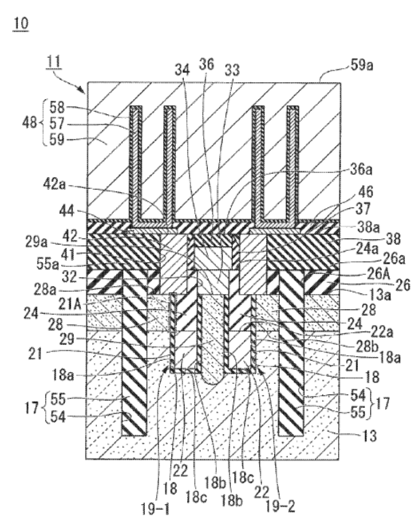
'597 Publication (published 2008)

FIG. 21



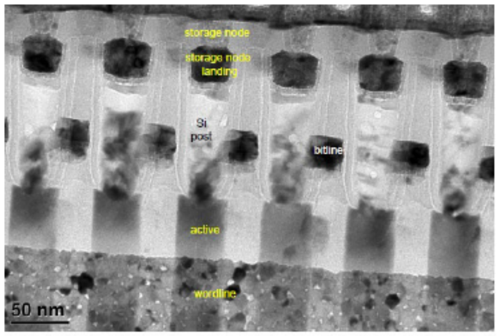
'407 Publication (Published 2010)

FIG. 2



'271 Publication (Published 2012)

This feature is also clearly visible in TEM images of commercially available DRAM devices obtained through reverse-engineering:



\3 TEM\wordline direction\storage node contact 64k_204861.png

Micron 2y nm SDRAM

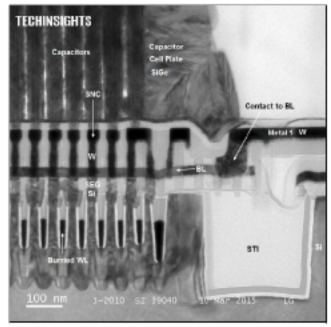


Figure 3.2.7: SDRAM storage node contacts, buried wordlines, and contact to bitline at the edge of SDRAM array, TEM cross section along bitline.

Samsung 20 nm SDRAM

(Chipworks Micron 2y Report at 16).

33. Dr. Liu similarly states with respect to the Elpida Process Document that page 55 "[redacted]" This page of the Elpida Process Documents, however, clearly demonstrates that the features identified by Dr. Liu can be seen in cross-sectional TEM images obtained through reverse-engineering:

[redacted]

Therefore, in my opinion the features identified by Dr. Liu in connection with the '162 Patent are not trade secrets because they would be readily ascertainable from reverse-engineering of commercially available DRAM products.

34. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '162 Patent were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '162 Patent describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

E. The '700 Patent

35. The '700 Patent generally discloses and claims a method of manufacturing a semiconductor device such as DRAM that involves forming storage node contacts by forming conductive patterns, and then forming isolation patterns between the conductive patterns, thereby simplifying the manufacturing process and increasing manufacturing yield. ('700 Patent at 1:31-36). This sequence of steps is shown in Figs. 4, 6, 8, 10, 12, and 14:

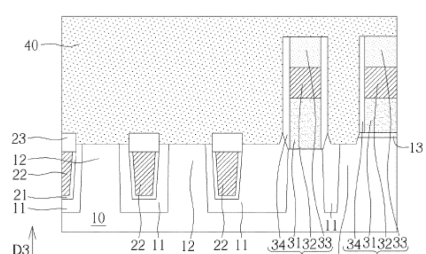


FIG. 4

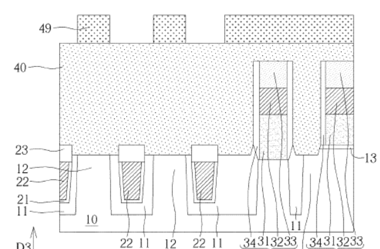


FIG. 6

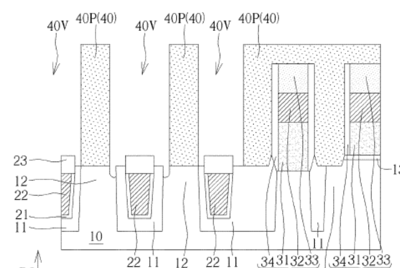


FIG. 8

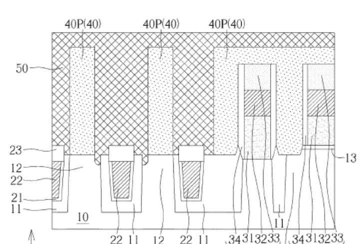


FIG. 10

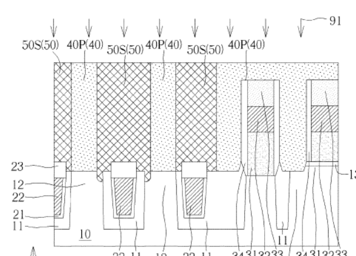


FIG. 12

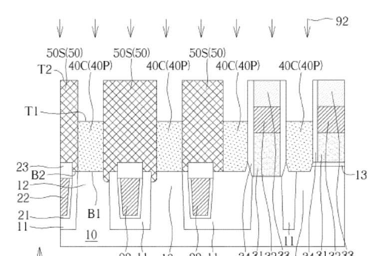


FIG. 14

In my opinion, the '700 Patent is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

36. Dr. Liu states with respect to the '700 Patent that "[redacted]" citing page 148 of the Micron 90 Series Traveler, and page 185 of the Micron 100 Series Traveler, as support. Dr. Liu also states with respect to the '700 Patent that "[redacted]

[redacted]" citing page 159 of the Micron 90 Series Traveler, and page 196 of the Micron 100 Series Traveler, as support. Finally, Dr. Liu states with respect to the '700 Patent that "[redacted]" citing pages 152 and 156 of the Micron 90 Series Traveler, and pages 189 and 192 of the Micron 100 Series Traveler, as support.

37. Contrary to Dr. Liu's assertions, the Micron/Elpida Process Documents show the opposite of the process disclosed and claimed in the '700 Patent. In particular, the Micron Process Documents show [redacted]:

[redacted]

[redacted]

Any reference by Dr. Liu to subsequent processing steps is highly misleading, since the ’700 Patent is clearly directed to the order in which the isolation structures above the bitlines, and the storage node contacts located therebetween, are formed.

38. For these reasons, I disagree with Dr. Liu’s opinion that “it is highly likely that the disclosures and purported inventions set forth in the ’700 Patent were derived from or based on Micron’s Confidential DRAM Technology …,” as well as his opinion that “[t]he ’700 Patent describes the same or very similar process technology as described in Micron’s Confidential DRAM Technology that I understand was in UMC’s possession.”

F. The ’205 Publication

39. The ’205 Publication generally discloses and claims a semiconductor device that includes a substrate, a plurality of memory cells, a plurality of contact plugs, and a bit line, where the contact plugs are physically and electrically connected to the bit line, and where the bottom surfaces of the contact plugs are lower than the surface of the substrate, as is shown in Fig. 10:

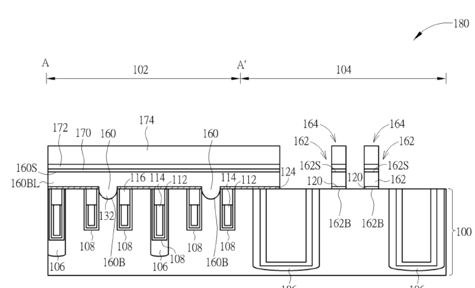


FIG. 10

('205 Publication at ¶ 5). In my opinion, the '205 Publication is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

40. Dr. Liu states with respect to the '205 Publication that "[redacted]" citing page 82 of the Micron 90 Series Traveler, and page 100 of the Micron 100 Series Traveler, as support. Dr. Liu also states with respect to the '700 Patent that "[redacted]" citing page 91 of the Micron 90 Series Traveler, and page 115 of the Micron 100 Series Traveler, as support. Finally, Dr. Liu states with respect to the '700 Patent that "[redacted]" citing page 95 of the Micron 90 Series Traveler, and page 117 of the Micron 100 Series Traveler, as support.

41. Contrary to Dr. Liu's statements, the Micron/Elpida Process Documents do not show [redacted]:

[redacted]

The features cited by Dr. Liu are, however, shown in the ’298 Publication, which was filed by Hynix on June 12, 2012, claiming priority to a Korean patent application that was filed on April 19, 2010, and which was published on October 18, 2012:

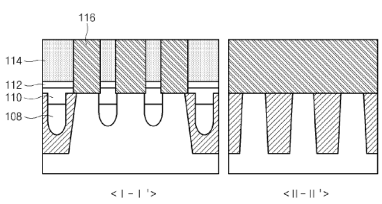


Fig.2

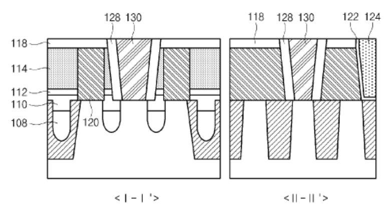


Fig.6

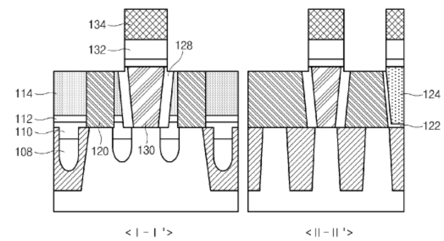


Fig.7

Therefore, in my opinion the features identified by Dr. Liu in connection with the ’205 Publication are not trade secrets because they would be readily ascertainable from publicly available information, including at least one United States published patent application.

42. For these reasons, I disagree with Dr. Liu’s opinion that “it is highly likely that the disclosures and purported inventions set forth in the ’205 Publication were derived from or based on Micron’s Confidential DRAM Technology …,” as well as his opinion that “[t]he ’205 Publication describes the same or very similar process technology as described in Micron’s Confidential DRAM Technology that I understand was in UMC’s possession.”

G. The ’563 Publication

43. The ’563 Publication discloses and claims methods for manufacturing an isolation structure, such as a shallow trench isolation (STI) structure, resulting in the top surface of the substrate having a flat or substantially flat appearance immediately after STI formation, which is beneficial for subsequent processing steps. (’563 Publication at ¶ 38). The claimed methods involve use of a plurality of hard mask layers, which are formed by different chemical vapor deposition processes so as to be stacked above an oxide layer formed on a substrate. (’563 Publication at ¶ 39). For two adjacent hard mask layers, the upper layer has a lower etching rate than the lower layer. (’563 Publication at ¶ 26). Consequently, during the patterning process, an upper hard mask layer pattern can be used to define a lower hard mask layer pattern. (’563 Publication at ¶ 26). In the disclosed embodiment, a first hard mask layer is an amorphous silicon layer, a second hard mask layer is an oxide layer, and a third hard mask layer is a two-layer stacked

structure comprising an organic dielectric layer and a silicon-containing hard-mask bottom anti-reflective coating. ('563 Publication at ¶ 27). In my opinion, the '563 Publication is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

44. Dr. Liu states with respect the '563 Publication that "[redacted]" citing pages 27-31 of the Micron 90 Series Traveler, and pages 25-30 of the Micron 100 Series Traveler, as support. He similarly states that "[redacted]" citing pages 27-28 of the Micron 90 Series Traveler, and pages 25-26 of the Micron 100 Series Traveler, as support. According to Dr. Liu, "[redacted]" citing page 36 of the Micron 90 Series Traveler, and page 38 of the Micron 100 Series Traveler.

45. Contrary to the assertions of Dr. Liu, the use of [redacted] is ubiquitous in the semiconductor industry, including in the DRAM industry, and this technique is necessary for obtaining small feature sizes due to limitations associated with photolithography. Double patterning processing steps are included in BKMs developed by semiconductor manufacturing equipment vendors such as AMAT and TEL and provided to customers who use their equipment. These companies typically teach their customers, including wafer fabs such as UMC, and DRAM manufacturers such as Micron, how to perform these processing steps. This was the case with UMC, who received detailed instructions on how to perform double patterning to form DRAM features such as STI regions from at least both AMAT and TEL: Since double patterning using sidewall spacers is known and used by virtually every semiconductor design company and wafer fab, in my opinion, the features identified by Dr. Liu with respect to the '563 Publication are not Micron trade secrets because they do not derive independent economic value from not being known to the general public. Moreover, in my opinion, UMC learned how to perform double patterning using sidewall

spacers from semiconductor manufacturing equipment vendors such as AMAT and TEL, not from any purported Micron trade secrets.

46. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '563 Publication were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '563 Publication describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

H. The '538 Publication

47. The '538 Publication discloses and claims methods for manufacturing an STI region in a manner that avoids damage to the active area of the device. ('538 Publication at ¶ 4). One disclosed method uses a first mask formed on the top surface of a single or stacked material layer formed on a substrate. ('538 Publication at ¶ 20). The first mask defines numerous openings that expose the top surface of the material layer. ('538 Publication at ¶ 20). A silicon oxide layer is deposited on this structure, covering the top surface and sidewalls of the first mask, and also covering the exposed top surface of the material layer. ('538 Publication at ¶¶ 20-22). Through multiple etching and deposition steps, sub-masks are formed that define trenches where the silicon oxide had been formed along the sidewalls of the first mask and subsequently removed. ('538 Publication at ¶¶ 20-24). Through further etching and deposition steps, STI trenches are formed between the sub-masks, and the STI trenches are filled with an insulating material to form STIs. ('538 Publication at ¶¶ 20-25). In my opinion, the '538 Publication is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

48. I understand that Dr. Liu has stated an opinion that "it is highly likely that the disclosures and purported inventions set forth in the '538 Publication were derived from or based on Micron's Confidential DRAM Technology." I also understand that Dr. Liu has stated an opinion that "[t]he '538 Publication describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession." I disagree.

49. Dr. Liu states with respect to the '538 Publication that "[redacted]" citing page 27 of the Micron 90 Series Traveler, and page 25 of the Micron 100 Series Traveler. Dr. Liu further states that "[redacted]" citing pages 29 and 31 of the Micron 90 Series Traveler, and pages 27 and 32 of the Micron 100 Series Traveler. Finally, Dr. Liu asserts that "[redacted]" citing page 31 of the Micron 90 Series Traveler, and page 32 of the Micron 100 Series Traveler.

50. As I have explained herein with respect to the '563 Publication, the use of double patterning is ubiquitous in the semiconductor industry, and double patterning processing steps typically are included in BKMs developed by semiconductor manufacturing equipment venders and provided to customers who use their equipment. This was the case with UMC, who received detailed instructions on how to perform double patterning from at least both AMAT and TEL. Therefore, in my opinion, the features identified by Dr. Liu with respect to the '538 Publication are not Micron trade secrets. Moreover, in my opinion, UMC learned how to perform double patterning using sidewall spacers from semiconductor manufacturing equipment vendors such as AMAT and TEL, not from any purported Micron trade secrets.

51. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '538 Publication were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '538 Publication describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

I. The ’657 Publication

52. The ’657 Publication generally discloses and claims an improved capacitor structure for use in a semiconductor device such as DRAM. (’538 Publication at ¶¶ 6-8). The capacitor structure includes a cylindrical lower electrode having a bottom portion that is recessed into a dielectric layer, is in contact with a storage node pad, and extends to a sidewall of the storage node. (’538 Publication at ¶¶ 6-8). The bottom portion of the cylindrical electrode has a first and second horizontal surfaces that are connected by a vertical segment, as is shown in Figs. 2 and 3 of the patent:

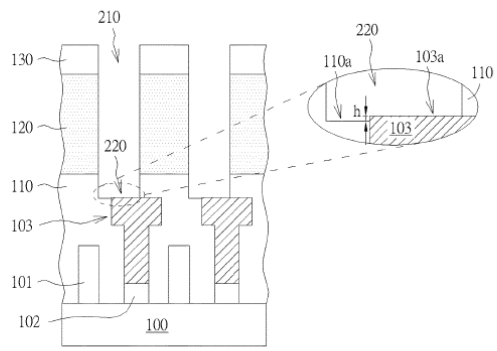


FIG. 2

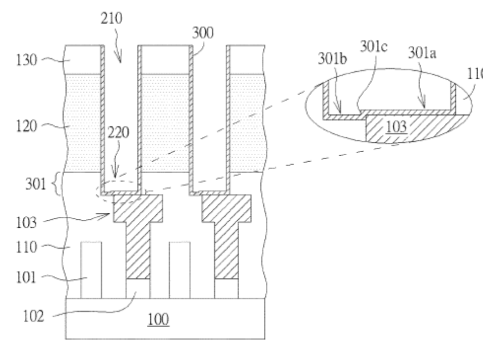


FIG. 3

(’538 Publication at ¶¶ 6-8). In my opinion, the ’657 Publication is not “based on,” is not “derived from,” and does not “describe” any Micron trade secrets.

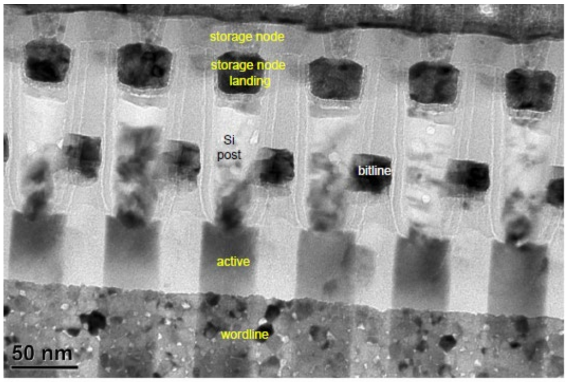
53. Dr. Liu states with respect the ’657 Publication that “[redacted]” citing page 197 of the Micron 90 Series Traveler, and page 240 of the Micron 100 Series Traveler, as support. Dr. Liu also states with respect the ’657 Publication that “[redacted]

[redacted]" again citing page 197 of the Micron 90 Series Traveler, and page 240 of the Micron 100 Series Traveler, as support. According to Dr. Liu, "[redacted]" citing pages 199-202 of the Micron 90 Series Traveler, and pages 242-251 of the Micron 100 Series Traveler.

54. Contrary to Dr. Liu's statements, however, the Micron/Elpida Process documents do not show an "[redacted]:

[redacted]

If this feature were present, however, it would be clearly visible in images obtained through reverse-engineering, such as the following TEM image prepared by Chipworks for a commercially available Micron Technology 2y nm GDDR5X SDRAM device, showing the storage node contact (*i.e.*, the "storage node landing"):



\3 TEM\wordline direction\storage node contact 64k_204861.png

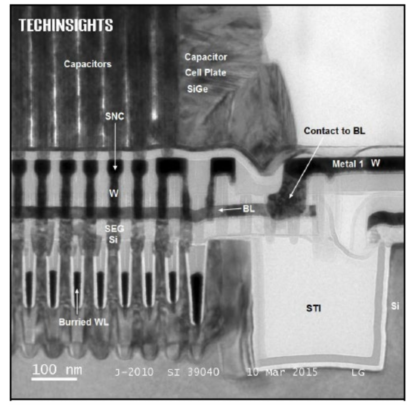


Figure 3.2.7: SDRAM storage node contacts, buried wordlines, and contact to bitline at the edge of SDRAM array, TEM cross section along bitline.

Micron 2y nm SDRAM **Samsung 20 nm SDRAM**

(Chipworks Micron 2y Report at 16). Therefore, in my opinion the features identified by Dr. Liu in connection with the ’657 Publication are not trade secrets because they would be readily ascertainable from publicly available information, including at least one United States published patent application.

55. For these reasons, I disagree with Dr. Liu’s opinion that “it is highly likely that the disclosures and purported inventions set forth in the ’657 Publication were derived from or based on Micron’s Confidential DRAM Technology …,” as well as his opinion that “[t]he ’657 Publication describes the same or very similar process technology as described in Micron’s Confidential DRAM Technology that I understand was in UMC’s possession.”

J. The ’863 Publication

56. The ’863 Publication discloses and claims methods for fabricating a capacitor, such as a capacitor used as a storage node in a DRAM device. (’863 Publication at ¶ 10). One method uses a first set of spacers SP1 formed of a spacer material such as silicon oxide and extending in a first direction D1 above an etch stop layer ES1, and a second set of spacers SP2 also formed of a spacer material such as silicon oxide and extending in a second direction D2 such that the second set of spacers SP2 intersect with the first set of spacers SP1. (’863 Publication at ¶¶ 10-16). In one embodiment, first and second directions D1 and D2 are perpendicular to one another, such that through holes defined by the first and second sets of spacers SP1 and SP2 are arranged in a rectangular pattern. (’863 Publication at ¶ 15). In another embodiment, first and second directions

D1 and D2 are at an acute angle with respect to one another, such that through holes defined by the first and second sets of spacers SP1 and SP2 are arranged in a hexagonal pattern. ('863 Publication at ¶ 16). In my opinion, the '863 Publication is not "based on," is not "derived from," and does not "describe" any Micron trade secrets.

57. Dr. Liu states with respect to the '863 Publication that "[redacted]" Dr. Liu cites pages 26, 230, 231, 234, and 237 of Micron's 100 Series Traveler as support for these assertions.

58. As I have explained herein with respect to the '563 Publication, the use of double patterning is ubiquitous in the semiconductor industry, and double patterning processing steps typically are included in BKMs developed by semiconductor manufacturing equipment venders and provided to customers who use their equipment. This was the case with UMC, who received detailed instructions on how to perform double patterning from at least both AMAT and TEL. Therefore, in my opinion, the features identified by Dr. Liu with respect to the '863 Publication are not Micron trade secrets. Moreover, in my opinion, UMC learned how to perform double patterning using sidewall spacers from semiconductor manufacturing equipment vendors such as AMAT and TEL, not from any purported Micron trade secrets.

59. For these reasons, I disagree with Dr. Liu's opinion that "it is highly likely that the disclosures and purported inventions set forth in the '863 Publication were derived from or based on Micron's Confidential DRAM Technology …," as well as his opinion that "[t]he '863 Publication describes the same or very similar process technology as described in Micron's Confidential DRAM Technology that I understand was in UMC's possession."

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

EXECUTED this 15th day of March 2019 at Palo Alto, California.

John E Berg

John Berg

EXHIBIT 1

TO THE DECLARATION OF JOHN BERG

JOHN BERG

• Palo Alto, California • 650.906.9657• ieeenano@gmail.com •

SUMMARY

As the Chief Technologist at American Semiconductor, Mr. Berg developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using double-gate FET technology. Before joining ASI, Mr. Berg developed automated tools for the nano-imprint industry at Transfer Devices. Prior to Transfer Devices, Mr. Berg was a Managing Director at Cypress Semiconductor, where he managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um. Mr. Berg is a MSEE candidate at University of California at Berkeley, focusing on analog CMOS circuit design, simulation, modeling, and process design. He did engineering and business graduate work at Stanford University. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology.

Mr. Berg has been an expert witness in semiconductor process development, silicon device physics, semiconductor design, CAD tools, and business practices. He served as the plaintiff's expert witness in the Palmchip v. Ralink (Mediatek) microprocessor patent infringement. He was an expert witness for the plaintiff Semi-Materials Co. Ltd. v. MEMC Pasadena Inc, in which he testified at jury trial twice and was deposed twice. In both cases, the plaintiff won, with more than $19M being awarded to Mr. Berg's client. Mr. Berg also has testified in front of the US Patent Office in the re-examinations of three patents, all of which were successfully defended, and has been an expert in numerous IPR cases. He was deposed as a Cypress employee in Cypress Semiconductor v. Altera Corp., where Altera was sued for interference with contract, trade secret misappropriation, and unfair competition involving programmable logic devices. At Standard Microsystems, he did reverse engineering analysis on competitors' products; these analyses led to three successful licensing agreements with other semiconductor companies.

PROFESSIONAL EXPERIENCE

BERG-ATTENBOROUGH, INC. **SEPTEMBER 2010 - PRESENT**

PRINCIPAL (2 EMPLOYEES)

Berg-Attenborough, Inc. is a consulting firm, which does technical consulting for Top 50 semiconductor companies and does expert witness work for patent and business issues.

Key Achievements:

- Fan-Out Wafer Level Packaging, FO-WLP consulting for Draper Laboratories (2015-1016)
- Successfully developed a 60+ chip multi-chip module including MPU, FPGA, DRAM, and FLASH. These were built with both flip-chip and wire-bonding techniques, on substrates, which used copper interconnect layers.
- Uncovered two major temperature cycle reliability problems with the existing FO-WLP technology, and instituted corrective actions to the process and design to eliminate these.
  - Modified interlayer dielectric and solder mask to correct die cracking
    - Problem uncovered by SEM and verified via SEM and reliability testing
  - Modified metal bus rules using Ansys and empirical data to ameliorate die cracking

• Palo Alto, California • 650.906.9657• ieeenano@gmail.com •

PROFESSIONAL EXPERIENCE (CONT.)

AMERICAN SEMICONDUCTOR, INCORPORATED **2005-2014**

CHIEF TECHNOLOGIST (22 EMPLOYEES)

American Semiconductor is fabricating radiation-hard CMOS products for military and aerospace customers.

Key Achievements:

- Hands-on in-fab development the front-end & back-end full wafer scale process for an antenna array product, which resulted in a Top Supplier of the Year Award from Boeing. A low temperature substrate-to-substrate bonding technique was developed specifically for this product.
- Hands-on in-fab development of the company's double-gate FET process, and successful transfer of the company's double-gate FET CMOS process from university laboratory into a CMOS production facility.
- Hands-on design for MCU/analog RF/sensor/memory flexible system-on-chip reference products:
    - Products includes hardware and software/firmware for system control and security/encryption
    - Process development included direct low temperature and high temperature direct wafer-to-wafer bonding techniques with and without through silicon vias (TSV's) to reduce system form factor.
    - Flip-chip, ball-bond, and wire-bonding used to assemble product.

TRANSFER DEVICES, SANTA CLARA, CA **2004-2005**

CHIEF OPERATING OFFICER (12 EMPLOYEES)

Transfer Devices is a lithography start-up, which is commercializing technology developed in Professor Fabian Pease's laboratory at Stanford University.

Key Achievements:

- Built a class 10 manufacturing clean room and delivered product to customers.
- Launched the ExaGlide 10r nano-patterning production tool development program
- Improved tool uptime from <10% to 95% and product yields from 50% to 99.9%

NANTERO, WOBURN, MA **2003-2004**

VICE PRESIDENT, NEW PRODUCT DEVELOPMENT (50 EMPLOYEES)

Nantero is developing non-volatile random-access memory using carbon nanotube switches.

Key Achievements:

- Hired and led the design team that taped out a 4Mb non-volatile memory chip, which resulted in a radiation-hardened non-volatile memory technology.

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PROFESSIONAL EXPERIENCE (CONT.)

CYPRESS SEMICONDUCTOR, SAN JOSE, CA **1998-2002**

MANAGING DIRECTOR, PROGRAMMABLE LOGIC (5500 EMPLOYEES)

Cypress Semiconductor, a public company, is a broad line supplier of semiconductor components.

Key Achievements:

- Program manager for Delta39K, 37K product lines, including hardware development, and software/firmware development on systems instantiated by customers.
- First Cypress multi-chip module product, using flip-chip and ball-bonding technologies.
- Hired, trained and managed the ESD team at Cypress (3 technology and design engineers). Reduced the number of corporate ESD-related design errors from 50% to <5% by standardizing ESD design rules, testing and incorporating secondary breakdown into the ESD design, standardizing ESD design methodology, and instituting formal ESD design reviews into Cypress's design flow. Purchased test systems for in-house ESD testing.
- Integrated NAND FLASH IC and SRAM-based CPLD IC into 1st Cypress multichip module
- Developed and put into production the company's 0.25um BiCMOS and 0.18um SiGe HBT processes used for the Company's Datacommunications Products.
    - Provided PDK, CAD, and Device support.
- Increased revenues from $38M to $72M by increasing the number of PLD/FPGA product families to 6, including the Ultra37000, Delta39K, Quantum38K and PSI product families
- Designed CPLD products in TSMC's 0.13um technology which used copper interconnect.

ZILOG CORPORATION NAMPA, ID **1990-1998**

VICE PRESIDENT, TECHNOLOGY DEVELOPMENT (1600 EMPLOYEES)

Zilog was a pre-IPO company that successfully went public in 1991, and was later acquired by IXYS.

Key Achievements:

- Trained and led the Nampa site's 15 person Design Department and 30 person Technology Development Department; delivered memory cells (SRAM, EEPROM, EPROM, NOR Flash), memory block compilers, and I/O cells for the company's design library for its system-on-chip and application-specific standard products. All products passed MIL-STD-883 reliability testing.
- Designed, built, and qualified the $175M 200mm fabrication facility; 1st silicon yield.
    - 0.25um CMOS technology, including CMP, tungsten plugs, trench isolation, and low k dielectric.
    - Solved the temperature cycle problem with the 200mm line within 90 days after initial observation. Solution involved modifying design rules for metallization.
- Hired, trained, and led the design team that taped out an average of 6 system-on-chip products per year for 8 years for the $120M Z8 microcontroller business unit.
- Worked with outside laboratories to ensure hardware design compliance to FCC's EMF/EMI requirements.
- Modified design rules and design clocking scheme to improve 1st pass yields.

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PROFESSIONAL EXPERIENCE (CONT.)

STANDARD MICROSYSTEMS CORPORATION, HAUPPAUGE, NY **1980-1990**
ENGINEERING DIRECTOR (500 EMPLOYEES)

Standard Microsystems was a public company in 1980, and later, was acquired by Microchip, Inc.

Key Achievements:

- Began career as a hands-on manufacturing CVD engineer working with Applied Materials deposition tools.
- Solved the company's Highly Accelerated Temperature/Humidity Stress Test (HAST) problem, that had been plaguing the company for five years, through the use of optimizing thin film dopant concentration.
- Instituted DOE and six sigma process development practices in 1986.
- Hired, trained, and managed 26 sustaining and development engineers in the company's 2500 wpm wafer fab. Developed and transferred five 2um/sub-2um CMOS technologies into production.
- Reversed engineered Intel, TI, and National Semiconductor products to provide evidence of infringement against Standard Microsystem's patents. This included working with and coordinating external laboratories to provide deconstruction analysis.

EDUCATION

2015-2019 **UNIVERSITY OF CALIFORNIA, BERKELEY** **BERKELEY, CA**
M.S., Electrical Engineering. Focus on heterogeneous analog, digital, and wireless products

2002-2003 **STANFORD UNIVERSITY** **PALO ALTO, CA**
M.S. Management, Graduate School of Business. Sloan Fellow.

1998-2002 **STANFORD UNIVERSITY** **PALO ALTO, CA**
16 graduate credits in Electrical Engineering (GPA = 4.1) in circuit design

1975-1980 **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** **CAMBRIDGE, MA**
BS Physics. Four-year National Merit Finalist and Scholar. Intercollegiate crew

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PUBLICATIONS

"MOS Transistor Technology from Planar to Nanowire Transistors," Mantha, B. and Berg, J., Silicon Valley Engineering Council Journal, Volume 1, 2009, Pages 23-32.

"Substrate Bias Effects on Transiently Triggered Latchup in Bulk CMOS," Chang, L. and Berg, J.; IEEE Transactions on Electron Devices, Volume 33, Issue 1, Jan. 1986 Pages 165 - 167

"A Derivative Method to Determine a MOSFET's Effective Channel Length and Width Electrically," Chang, L. and Berg, J.; IEEE Electron Device Letters, Volume 7, Issue 4, Apr 1986 Pages 229 – 231.

"A Simplified Model to Predict the Linear Temperature Coefficient of a CMOS Inverter's Delay Time," Chang, L., Khoa Vo and Berg, J.; IEEE Transactions on Electron Devices, Volume 34, Issue 8, Aug 1987 Pages 1834 – 1837.

CONFERENCE LEADERSHIP AND PRESENTATIONS

Co-Chairman, 2007 IEEE San Francisco Bay Area Nanotechnology Symposium, July 2007.

"Rad-Hard Reconfigurable Bidirectional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet 0.18um SOI CMOS Technology," K. DeGregorio, D. Wilson, S. Parke, J. Berg, M. Goldston, R. Hayhurst, D. Hackler 12th NASA Symposium on VLSI Design

Committee Member, Programmable Logic Sub-Committee, 2003 IEEE Solid State Circuits Conference, San Francisco, CA

"Measuring the Effective Channel Length of the Deep Submicron MOSFET and the Channel Broadening Effect," S.H. Chung, Tim Carns, S.K. Lee, L. DeBruler, and J. Berg, Proceedings of the Thirteenth Biennial University/Government/Industry Symposium, IEEE Press, pp. 176-181, 1998.

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PATENTS

Patent Number	Title
8,913,402	Triple-damascene interposer
7,595,527	Non-volatile electromechanical field effect devices and circuits and methods of forming same
6,476,635	Programmable number of metal lines and effective metal width along critical paths in a programmable logic device
6,436,195	Method of fabricating a MOS device
6,190,973	Method of fabricating a high quality thin oxide
6,165,846	Method of eliminating gate leakage in nitrogen annealed oxides
6,156,653	Method of fabricating a MOS device
5,978,127	Light Phase Grating Device
5,631,180	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,498,896	High threshold metal oxide silicon read-only-memory transistors
5,389,565	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,338,423	Method of eliminating metal voiding in a titanium nitride/aluminum processing
5,317,187	Ti/TiN/Ti contact metallization
5,244,831	Method of doping a polysilicon layer on a semiconductor wafer
5,240,880	Ti/TiN/Ti contact metallization
4,895,520	Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant
4,824,803	Multilayer metallization method for integrated circuits

PROFESSIONAL MEMBERSHIPS

• National Science Foundation, Electronics & Nanotechnology Phase I & II SBIR Reviewer •
• Gerson, Lehrman Group: Leader (Top 5%) Council member •
• Chair Emeritus, and Founding Member, IEEE San Francisco Bay Area Nanotechnology Council •
• IEEE National Chapter of the Year Award, 2013 •
• Executive Committee Member, IEEE Santa Clara Valley Section •
• Member, Silicon Valley Engineering Council Steering Committee •
• Senior Member, IEEE •
• Member, Sigma Xi •
• Member, New York Academy of Science •
• Chair, Vistage International 2010-2015 •
• Security Clearance: Secret •

SEMINARS, TUTORIALS & WORKSHOPS

• ESD Association Tutorial: "Prevention of Electrostatic Discharge to Electronic Devices, Assemblies, and Systems." 1998 •
• Juran Institute, "Juran Management Systems," 1989 •

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SOFTWARE

DESIGN TOOLS:

SYNOPSYS: GALAXY DESIGN PLATFORM: DESIGN COMPILER, CUSTOM DESIGNER SE/DE/SDL, PRIMETIME, IC COMPILER, HSPICE, IC VALIDATOR, POWER COMPILER

CADENCE: AMS DESIGNER, ASSURA, SPECTRE, VIRTUOSO

MENTOR GRAPHICS: CALIBRE

TCAD:

SILVACO: ATHENA, ATLAS, VICTORY

OTHER TOOLS: VHDL, PYTHON, JSON, JMP, MATLAB, MICROSOFT OFFICE SUITE